



H77H2-EM

Rev : A

ECS
CONFIDENTIAL

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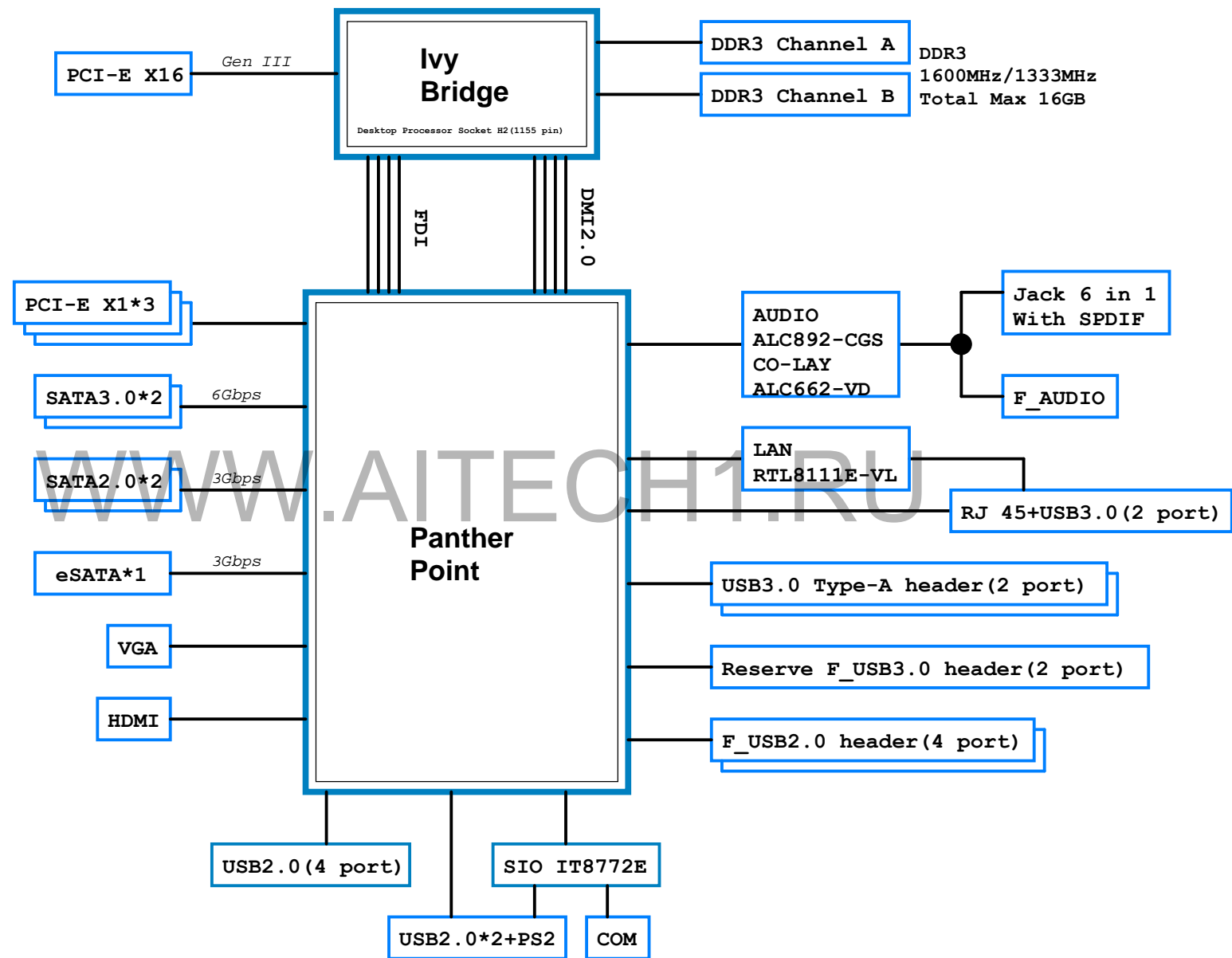
NOTE:
Design by
29517_29517_Maho_Bay_and_PDG_Rev0_7.pvd
29057_29057_Panther_Point_EDS_29057,0.5v1.pvd
MahoBay_Schematic_Rev0p70.pdf

REVISION HISTORY:

Rev	Date	Notes
V.A	2011/XX/XX	Base on MRS of H77H2-EM (2011-XX-XX)
V.A	2011/05/26	Modify from H77H2-LM V.B (2011-05-16)
V.A	2011/08/29	Modify ISL6363 for Nph=4 to Nph=3.

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Elitegroup Computer Systems		
Title Cover Page		
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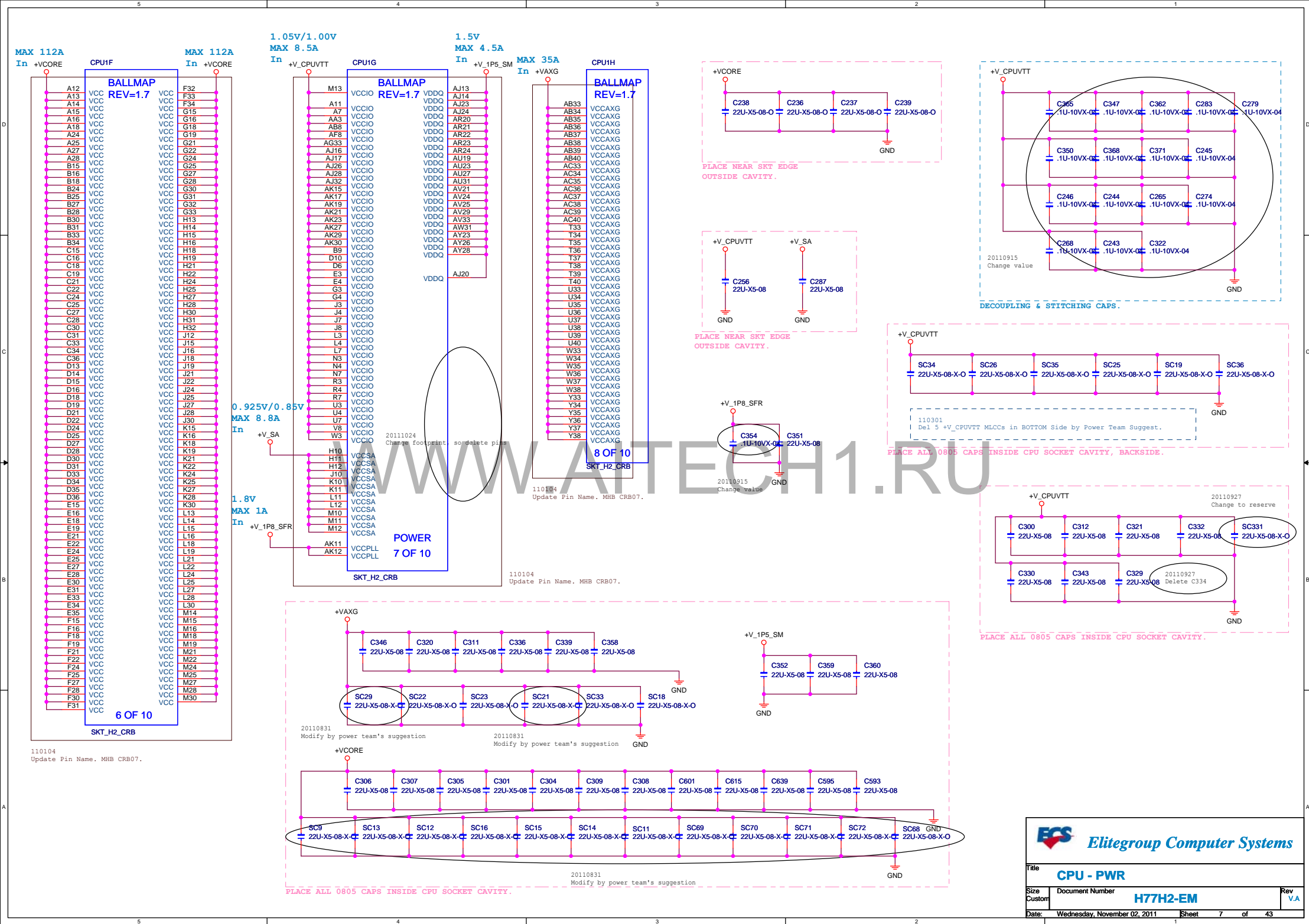
PCH-GPIO function

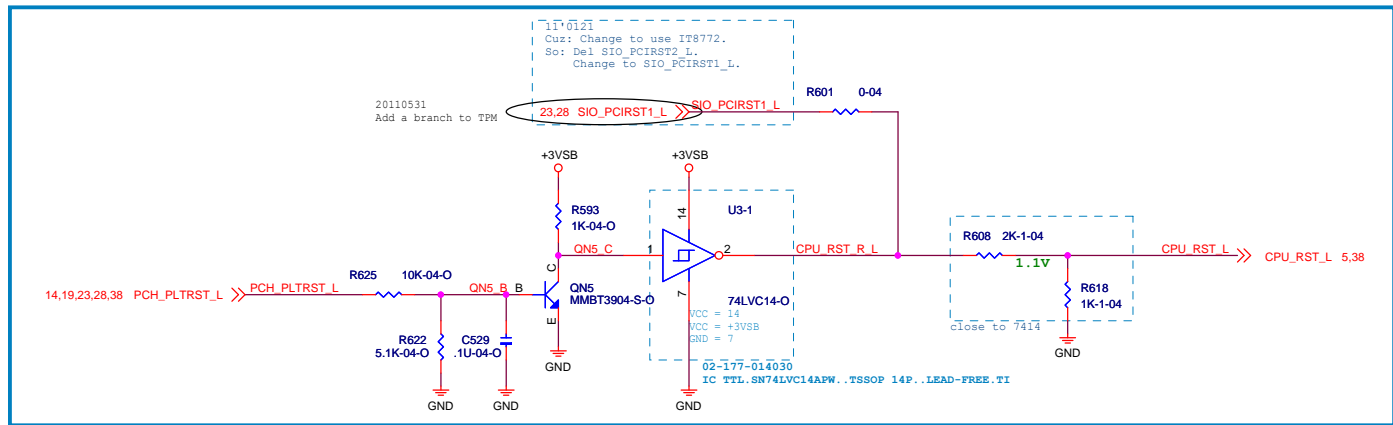
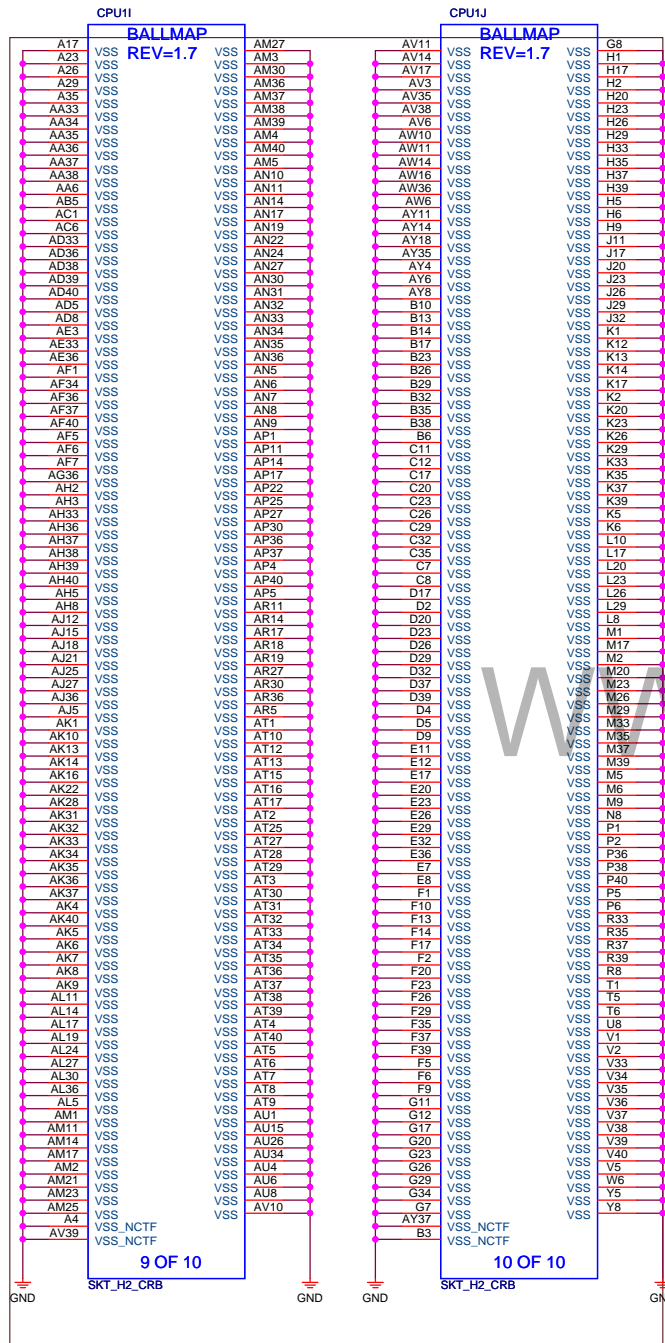
Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	GP1_BOMDET2	GPI
GPIO6	VCC3	GP6_BOMDET3	GPI
GPIO7	VCC3	GP7_BOMDET4	GPI
GPIO9	3VSB	USB_OC_L5	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO13	3VSB	LPC_PME	GPI
GPIO14	+DIMM_5VDUAL	PCH_LED1	Native
GPIO17	VCC3	GP17_BOMDET1	GPI
GPIO21	VCC3	GPIO21_COM2_DET	GPI
GPIO22	VCC3	CLR_CMOS_GP22	GPI
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO39	VCC3	GPIO39_CASE0	GPI
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO45	3VSB	WLAN_DIS_L	Native
GPIO48	VCC3	GPIO48_CASE1	GPI
GPIO59	3VSB	USB_OC_L0	Native
GPIO72	3VSB	GPIO72_BOMDET5	Native

SIO-GPIO function

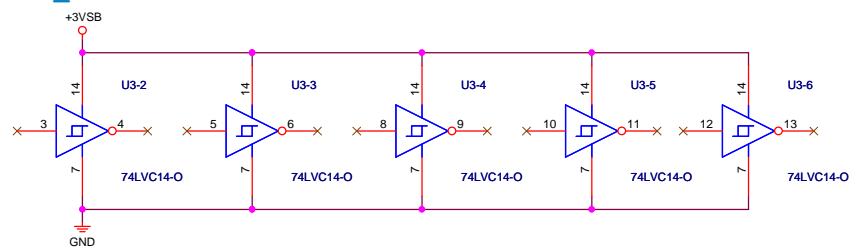
Pin Name	Power Well	Usage	Default Status
GP10	3VSB	SIO_PCIRST3_L	PCIRST3#
GP12	VCC3	SIO_PCIRST1_L	PCIRST1#
GP22	3VSB	SIO_LED0	GP22
GP23	3VSB	DPWROK	CPU_PG
GP30	VCC3	ATXPWRGD	ATXPWRGD
GP31	VCC3	CTS1_L	CTS1#
GP32	VCC3	SIO_RI1_L	RI1#
GP33	VCC3	DCD1_L	DCD1#
GP36	VCC3	FAN_CTL2	FAN_CTL3
GP37	VCC3	FAN_TAC2	FAN_TAC3
GP40	3VSB	GPIO40_S4S5	3VSBSW#
GP41	3VSB	SIN1	SIN1
GP42	3VSB	PSON_L	PSON#
GP43	3VSB	FP_PWRBTN_L	PANSWH#
GP44	3VSB	SIO_PWRBTN_L	PWRON#
GP45	3VSB	DSR1_L	DSR1#
GP51	VCC3	FAN_CTL1	FAN_CTL2
GP52	VCC3	FAN_TAC1	FAN_TAC2
GP53	3VSB	SLP4_L	SUSC#
GP54	3VSB	LPC_PME_L	PME#
GP55	3VSB	RSMRST_L	RSMRST#
GP56	3VSB	MCLK	MCLK
GP57	3VSB	MDATA	MDAT
GP60	3VSB	KCLK	KCLK
GP61	3VSB	KDATA	KDAT
GP62	VCC3	KBRST_L	KRST#
GP65	3VSB	SMLK1_SIO_DATA	VLDT_EN

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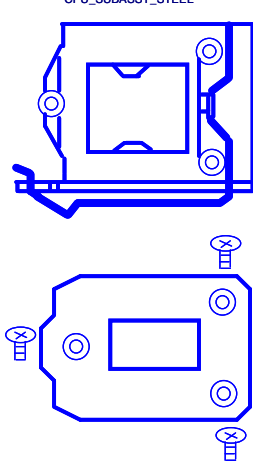


PLTRST_L Driving Circuit



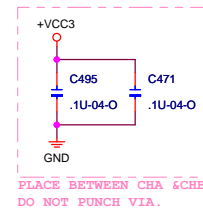
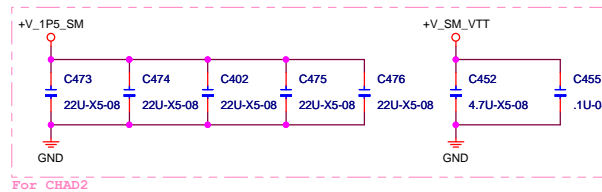
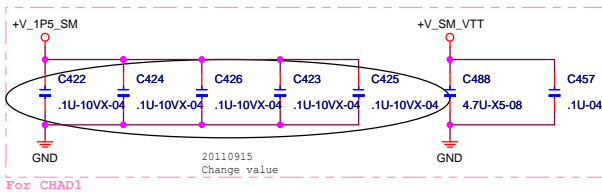
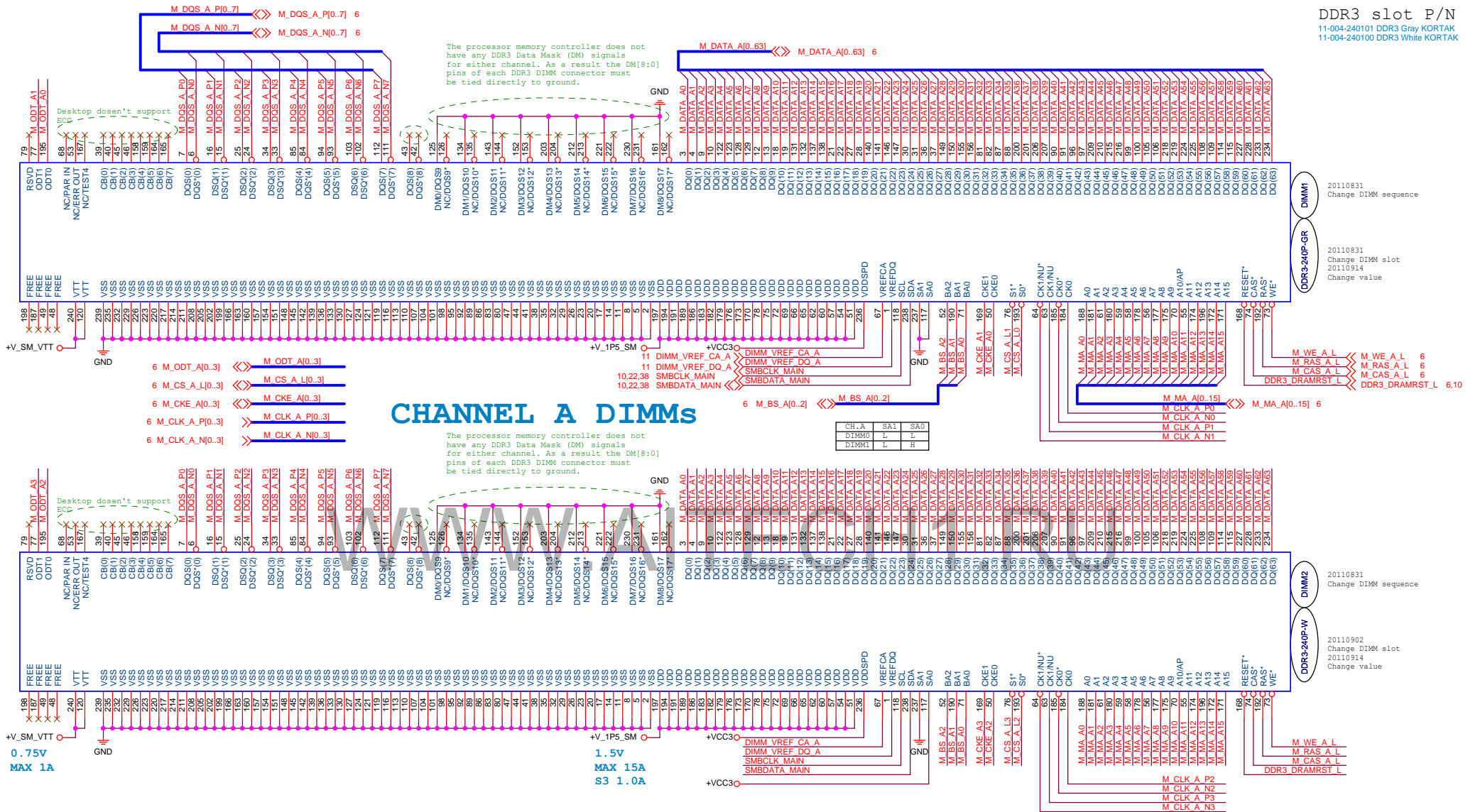
WWW.AITECH1.RU

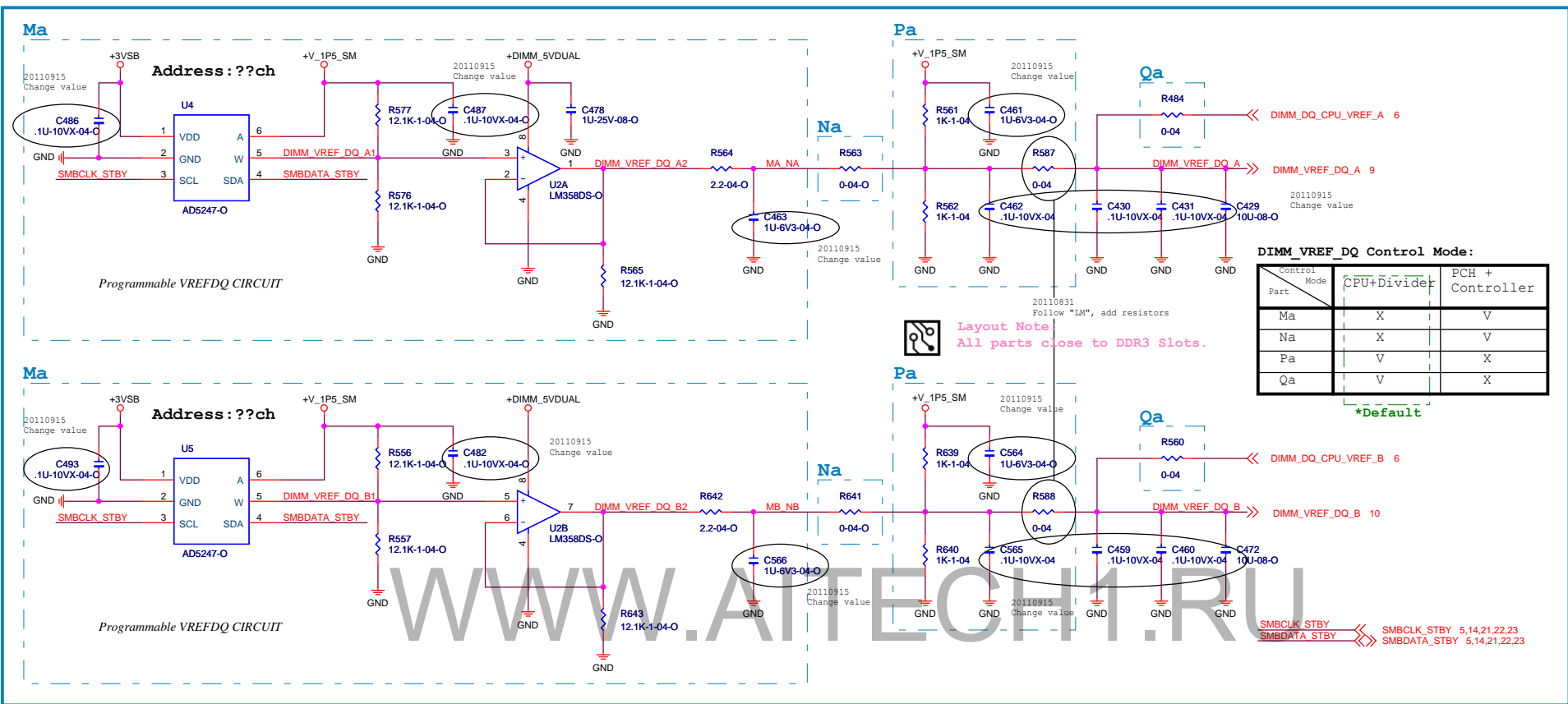
CPU steel P/N
 20-800-004611
 SUBASSY_STEEL...LGA 1156P
 W/BACK PLATE.ACA-ZIF-082-K01....LEAD-FREE (RoHS) .LOT#S



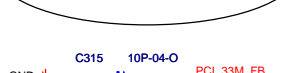
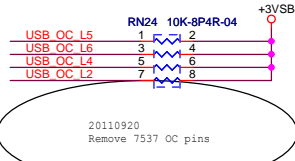
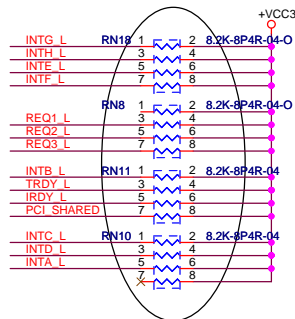
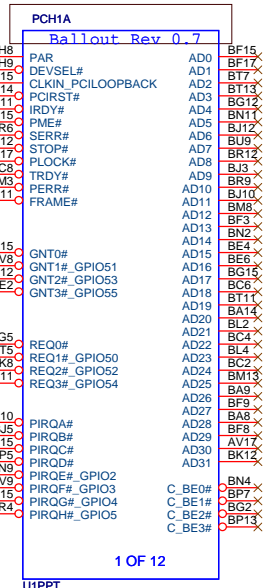
CPU socket P/N
 11-018-115124
 SOCKET.CPU..LGA 1155P SMD..G/F
 BLACK.ACA-ZIF-096-P02....LEAD-FREE (RoHS/HP) .LOT#S



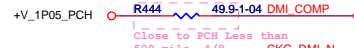




110104
Update Pin Name, MHB CRB07.



20110831
Follow "LM"
Change to 0402
2011025
Modify



PCIE1X_3 Slot

PCIE1X_1 Slot

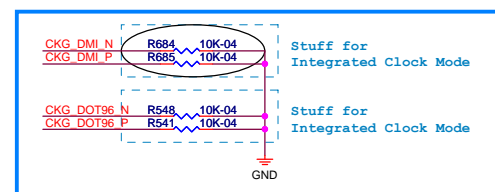
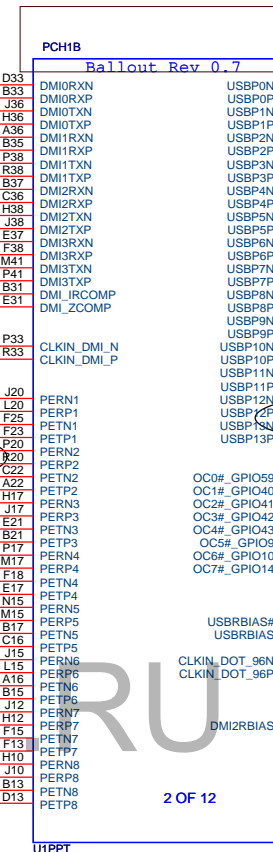
PCIE1X_2 Slot

Giga Lan Controller

20110831
Follow "LM", change port for INT# issue

20110927
Remove SC73, SC74

110104
Update Pin Name, MHB CRB07.

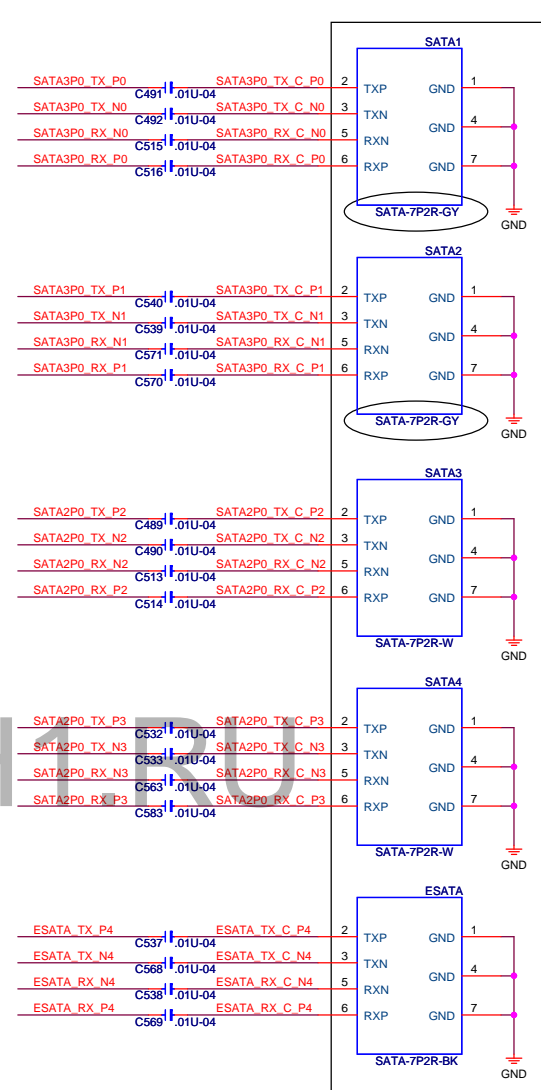
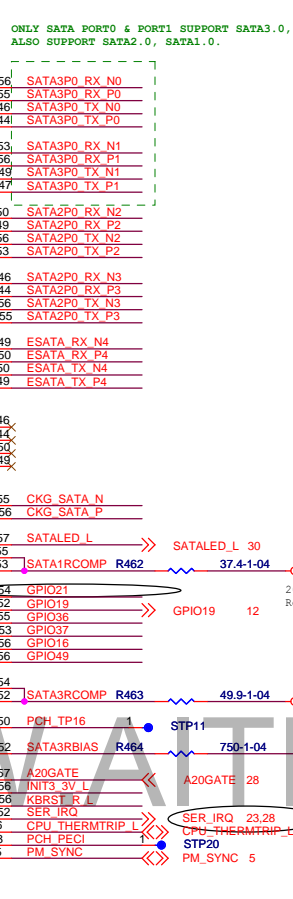
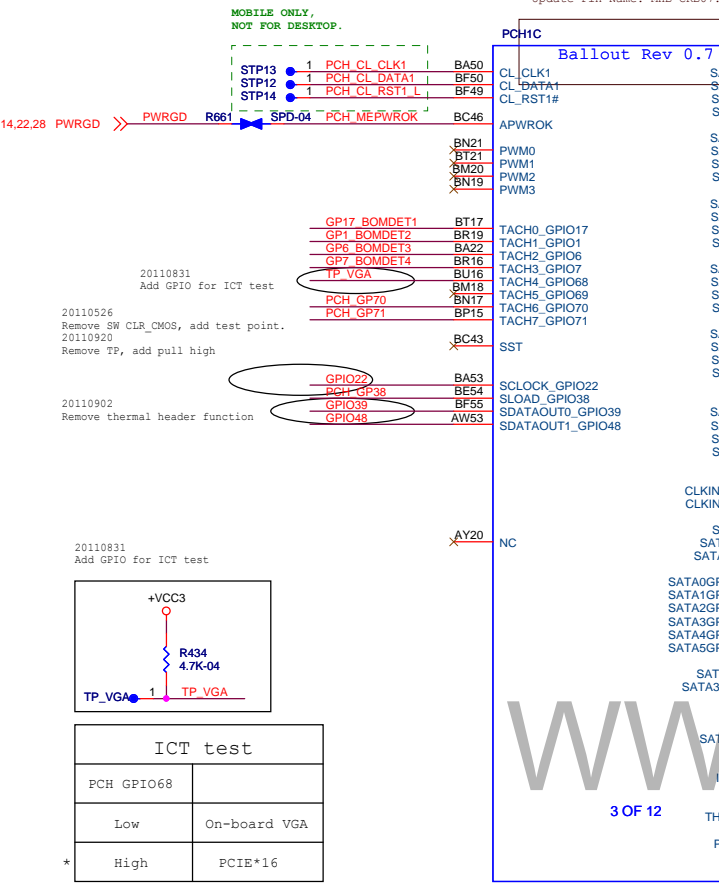


Function	INT port	PCI-E X1 port	Chipset
LAN Ethernet Controller	INTA#	PCI Express #7 Pin	Realtek RTL8111E
SATA Controller	INTB#	N/A	H77 integrated

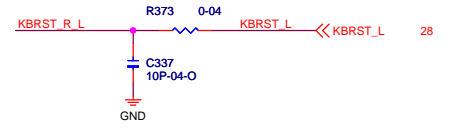
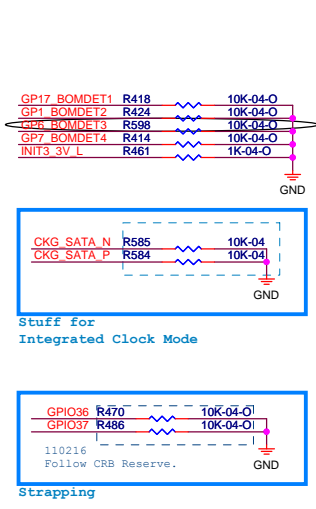
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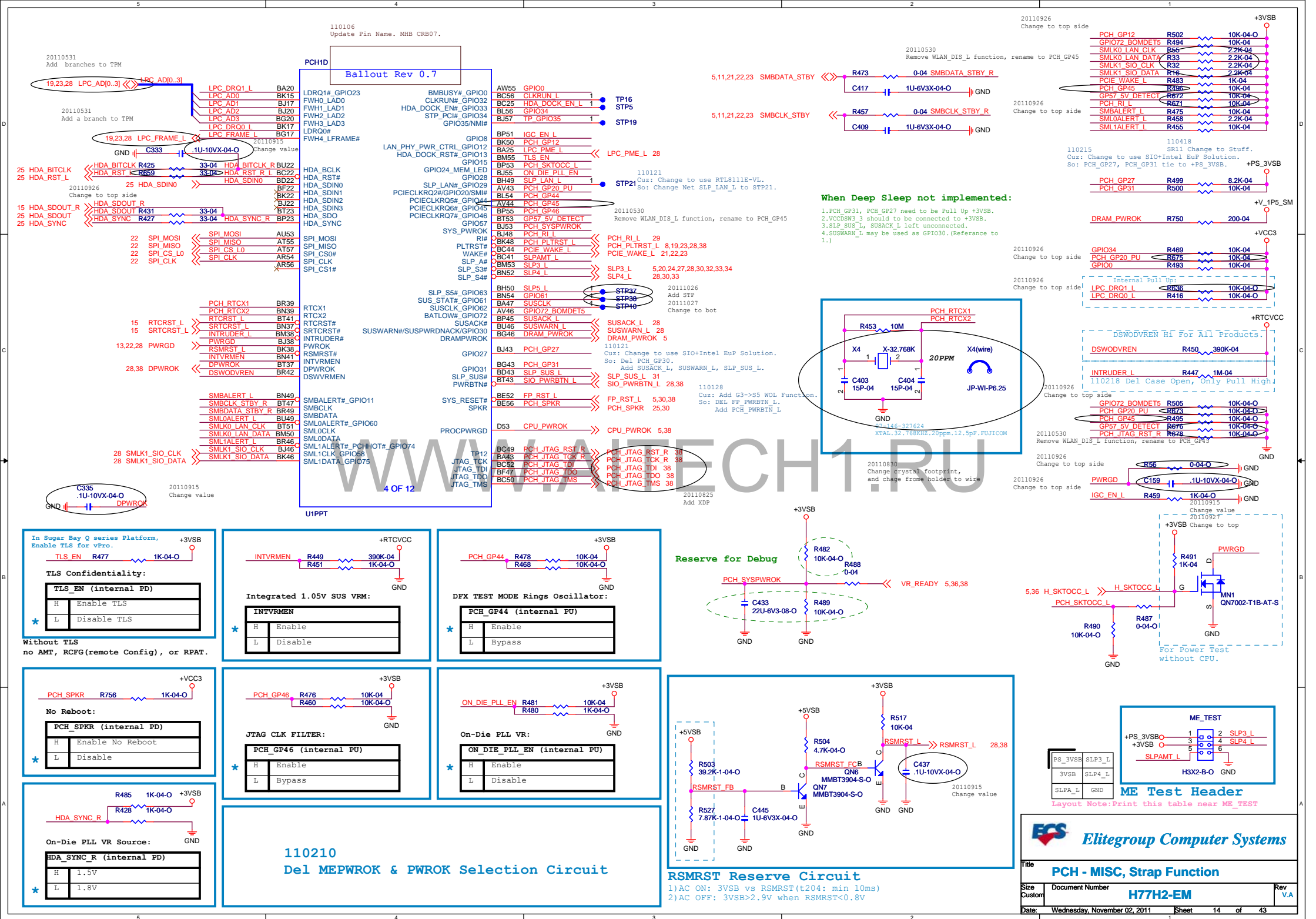
Title PCH - DMI/PCH-PE/USB			
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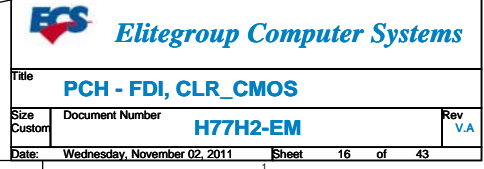
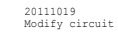
MOBILE ONLY, NOT FOR DESKTOP.

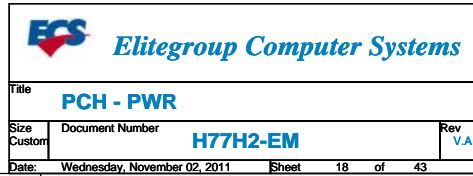


Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%

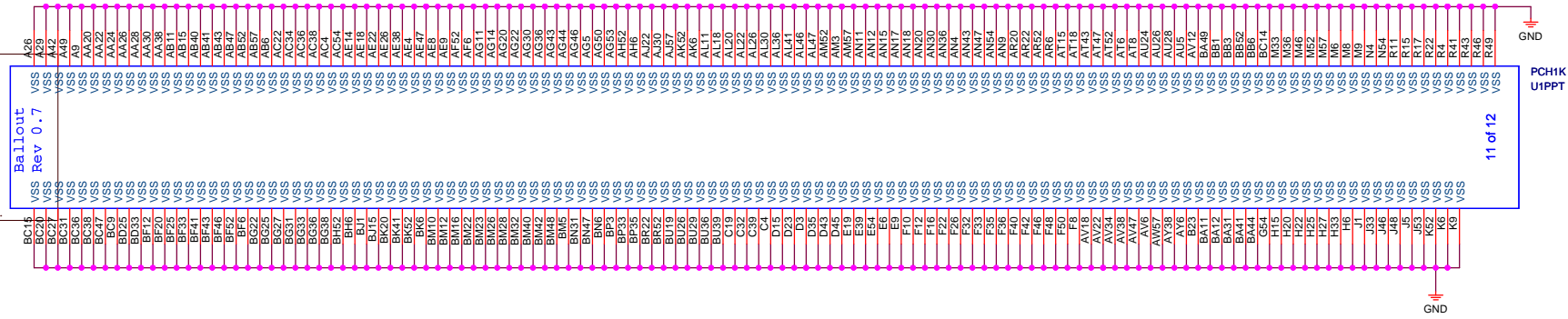




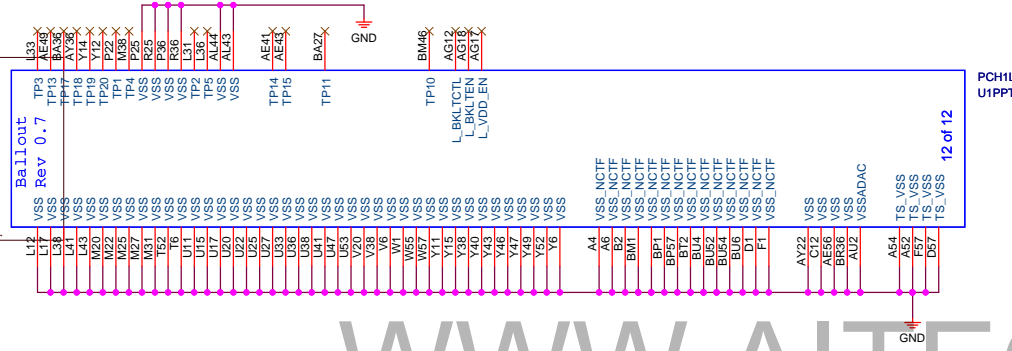




110106
Update Pin Name. MHB CRB07

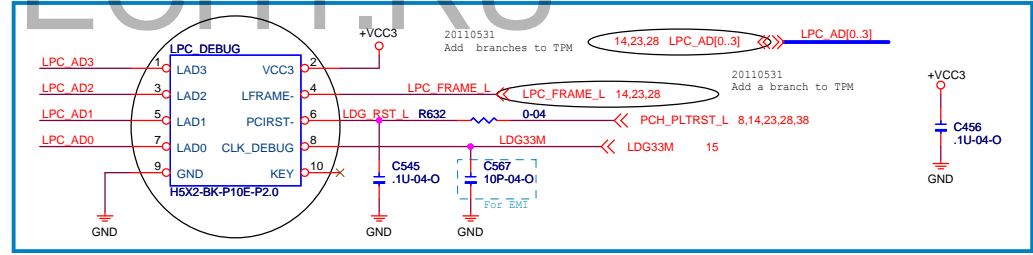


110106
Update Pin Name. MHB CRB07

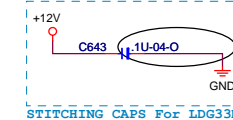


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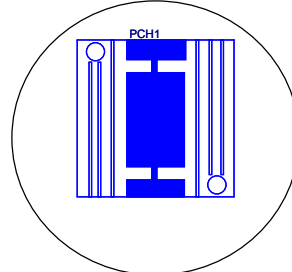
20110921
Change footprint



LPC Debug header Circuit



20110915
Change value
20110920
Change to Y5V



20110829
Change PCH heatsink
20110914
Change footprint

20110830
Change holes pin define
20111027
Change footprint

PCI-E SPEC:
VCC3-->3A
12V-->5.5A
3VSB-->0.375A

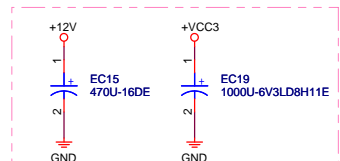
5,11,14,22,23 SMBCLK_STBY
5,11,14,22,23 SMBDATA_STBY

14,22,23 PCIE_WAKE_L



20110920 04-884-224103
Change value C/C,0.22uF,16V,10%,X5R...SMD 0402

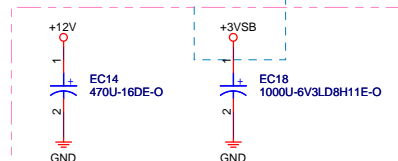
04-711-102073
E/C.1000uF,16V,20%...105C,RT D10*17mm....



Between PEX16 & PEX1A

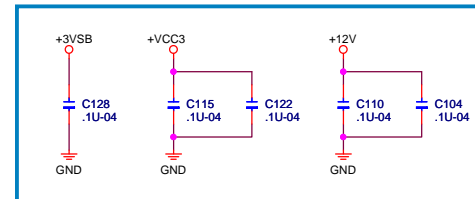
20110914
Change value

04-711-102073
E/C.1000uF,16V,20%...105C,RT D10*17mm....



Between PEX1A & PEX1B

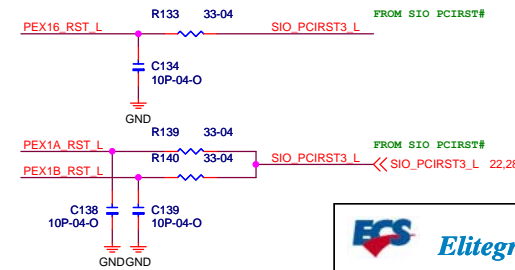
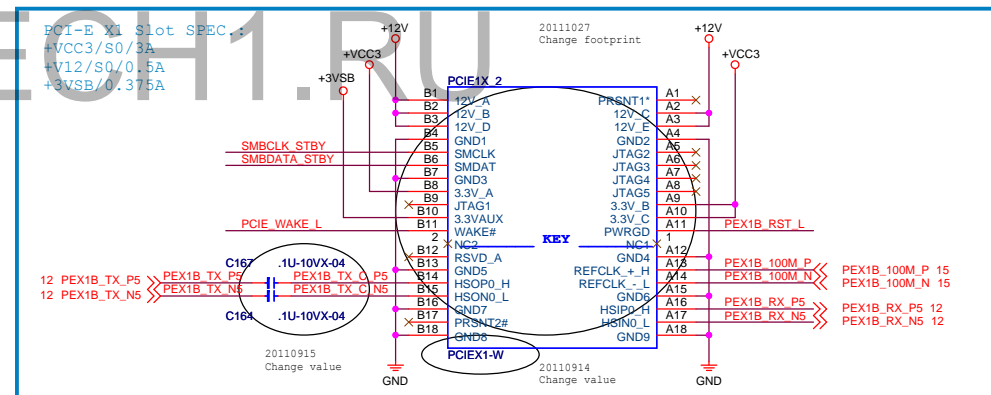
PCI-E X1 A



PCI-E X1 A Decoupling Cap.

PCI-E X1 B Decoupling Cap.

PCI-E X1 B



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Title	Slot - PCI-EX16/PCI-EX1	Rev	VA
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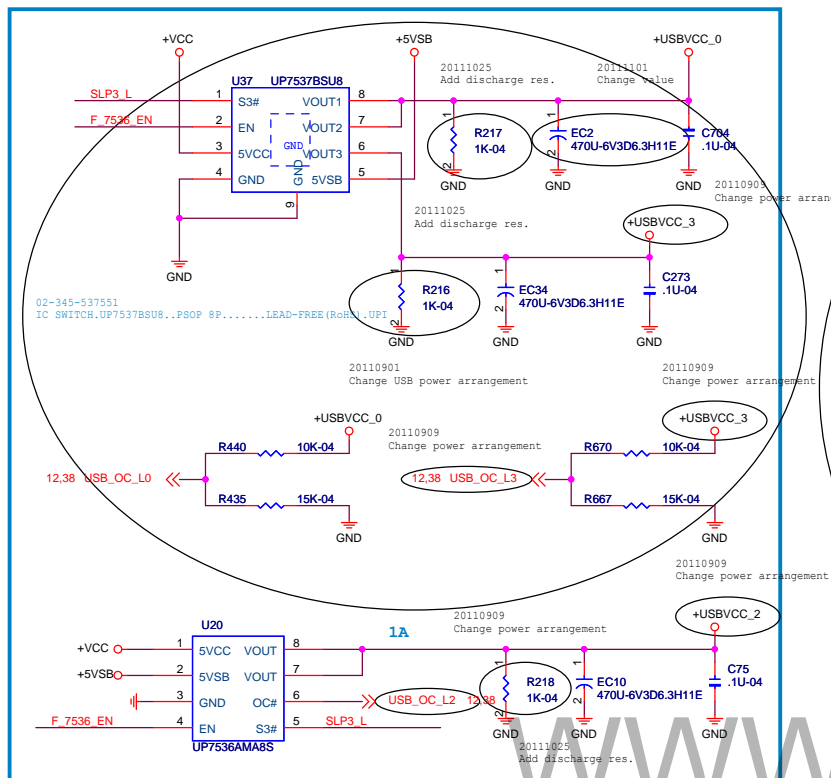
PCI-E X1 C

PCI-E X1 C Decoupling Cap.

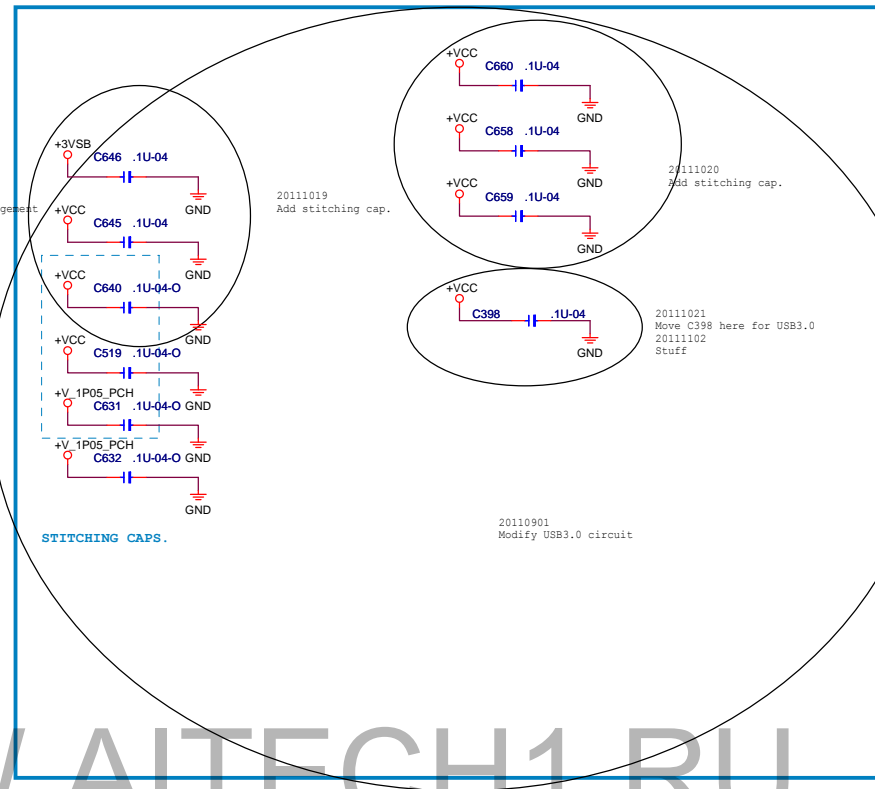
Between PEX1B & PEX1C

SMBUS Logic Circuit

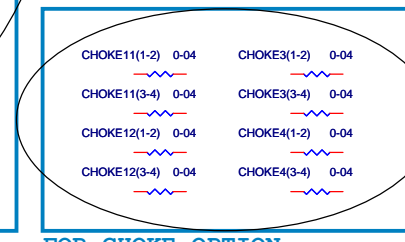
SPI ROM Circuit



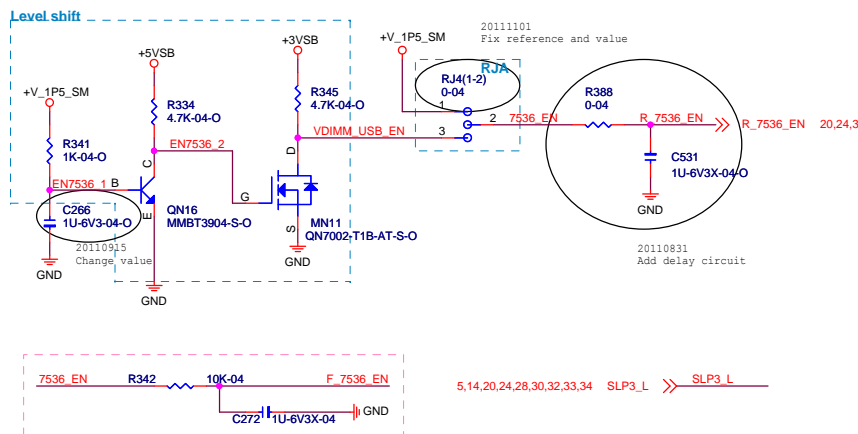
USB2.0/3.0 POWER CIRCUIT.



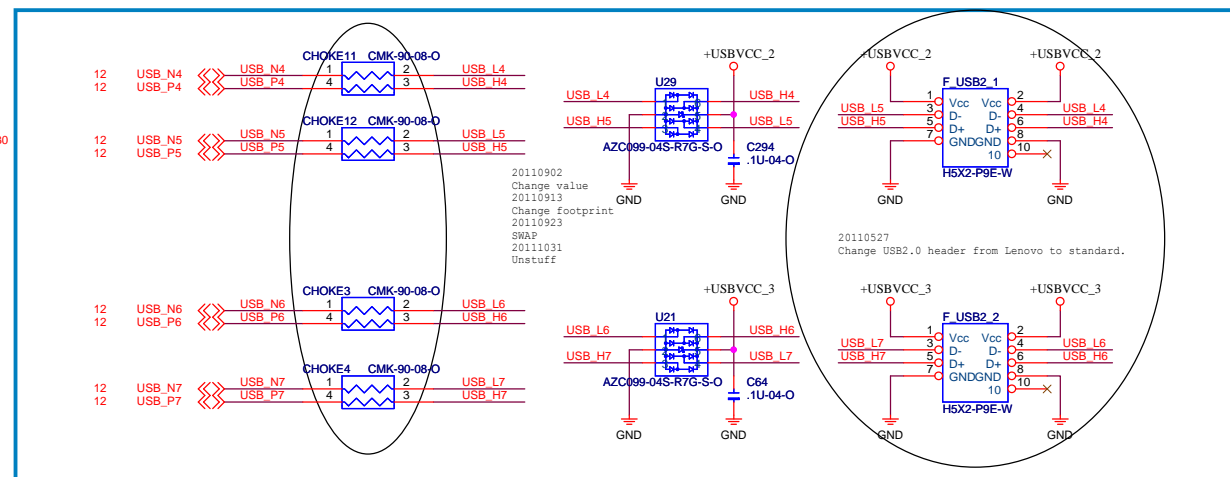
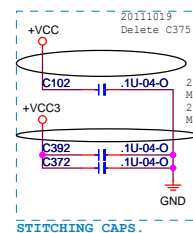
FRONT SIDE 2 PORTS USB3.0 Header



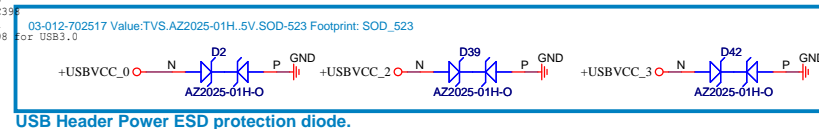
FOR CHOKE OPTION

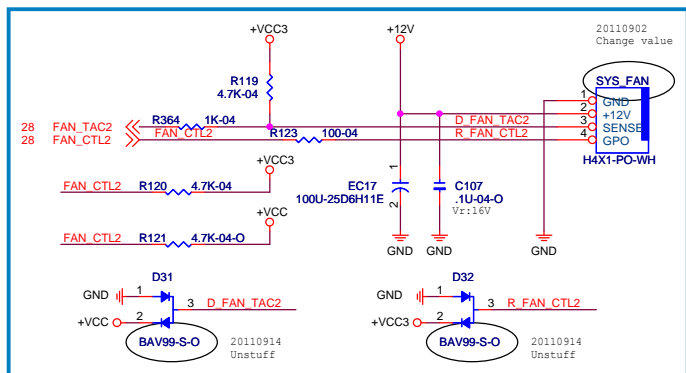


uP7536 Enable use	Level shift	RJA	RJB	S4/S5 USB_5V_DUAL	Customer
VDIMM	N A	0ohm (1-2)	N A	0 Volt	Lenovo
VDIMM level shift (3.3V)	Stuff	0ohm (2-3)	N A	0 Volt	S4/S5 w/o USB_5V_DUAL

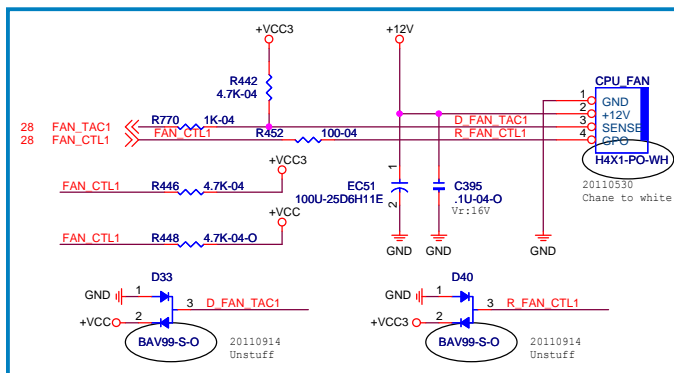


FRONT SIDE 4 PORTS USB2.0 Header

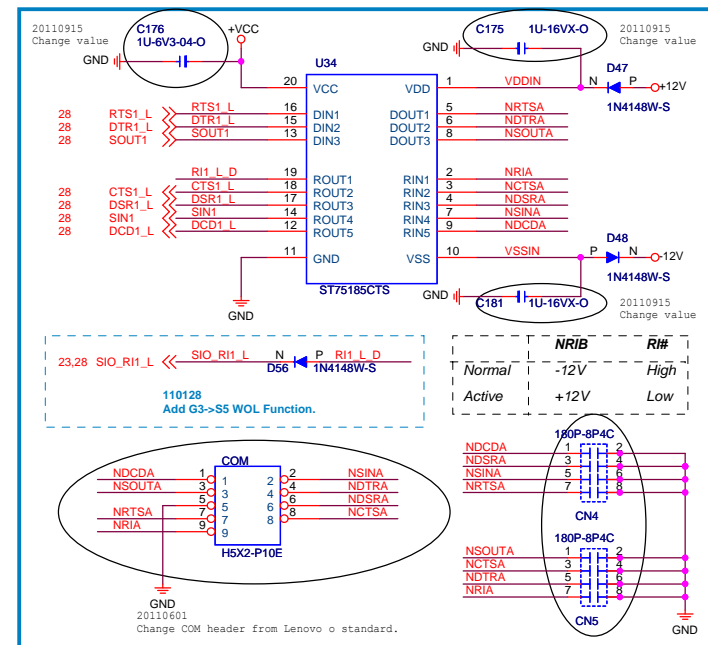




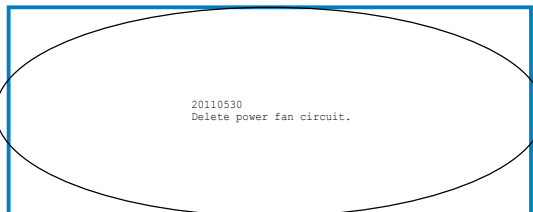
SYS_FAN 4-PIN Circuit



CPU_FAN 4-PIN Circuit



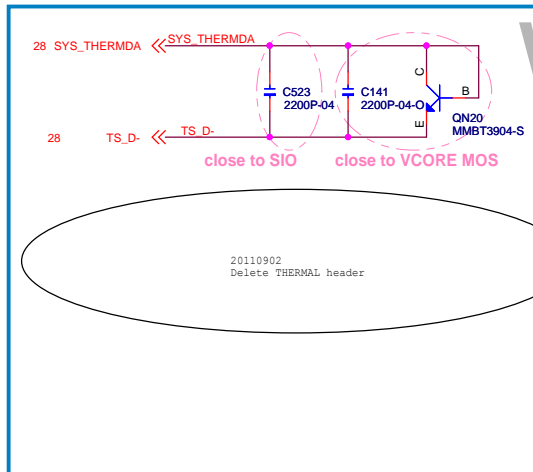
COM Header Circuit



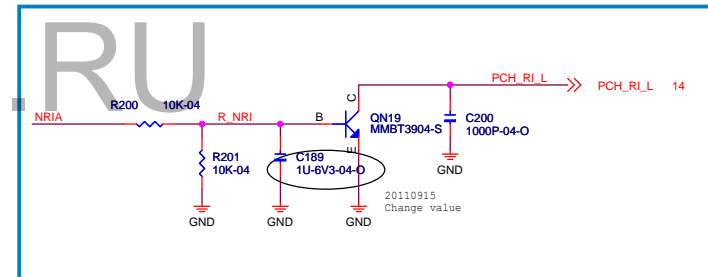
PWR_FAN 3-PIN Circuit



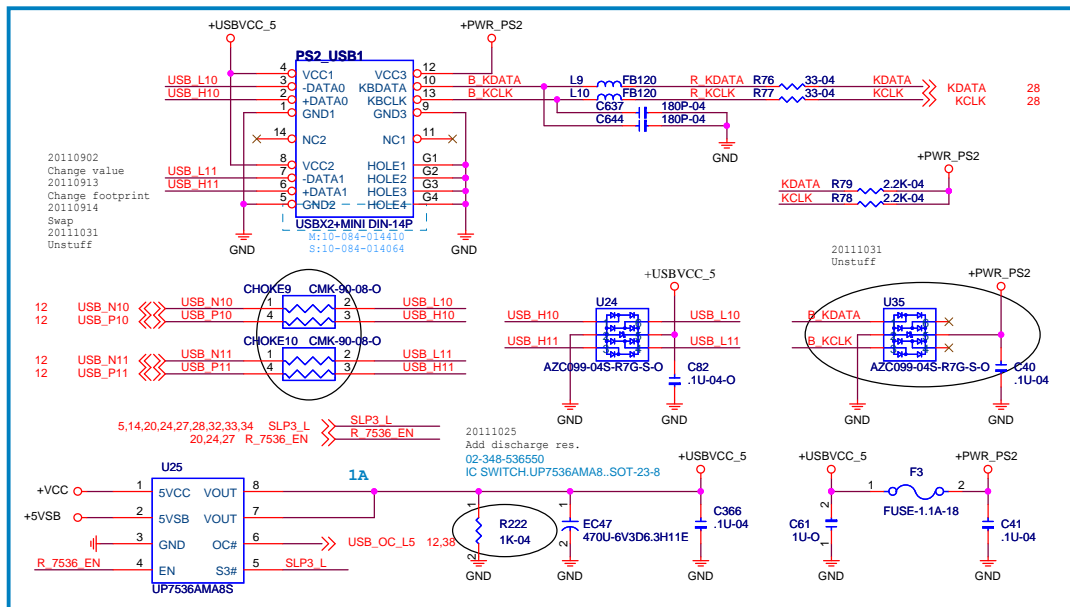
CASE Open Circuit



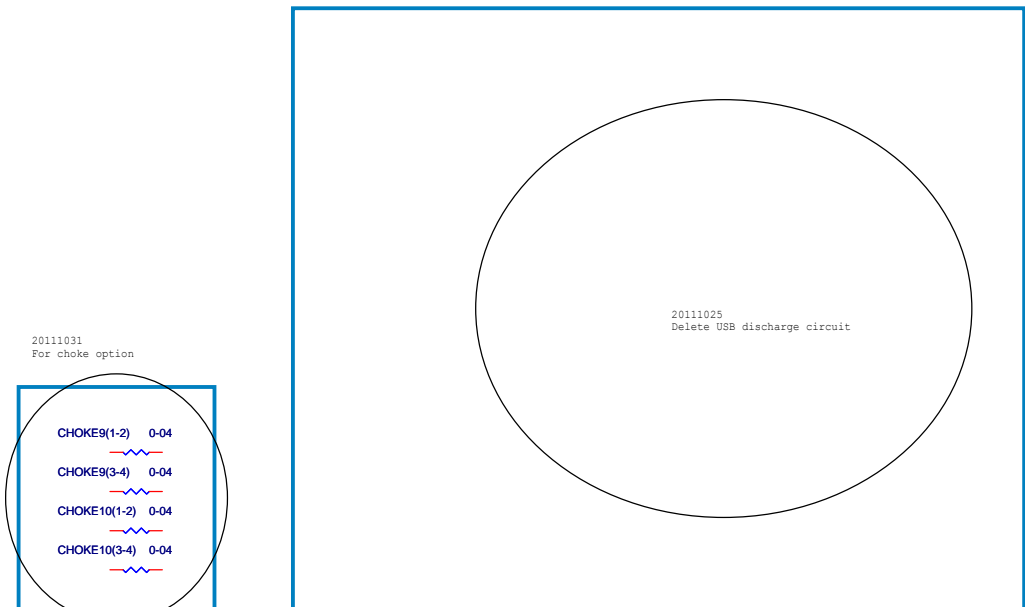
Thermal Sense



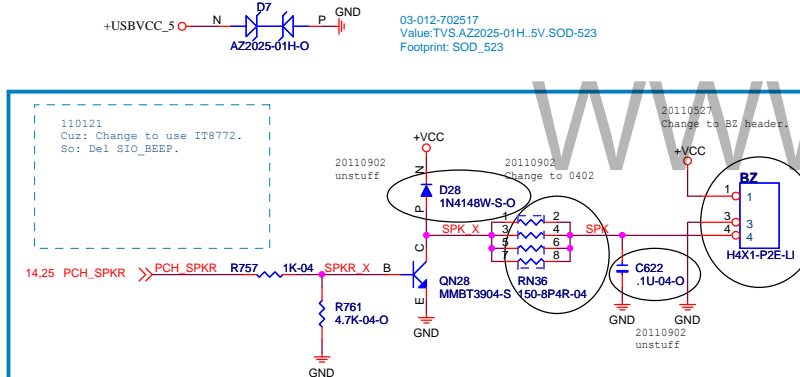
COM2 RI# Wake Up Circuit



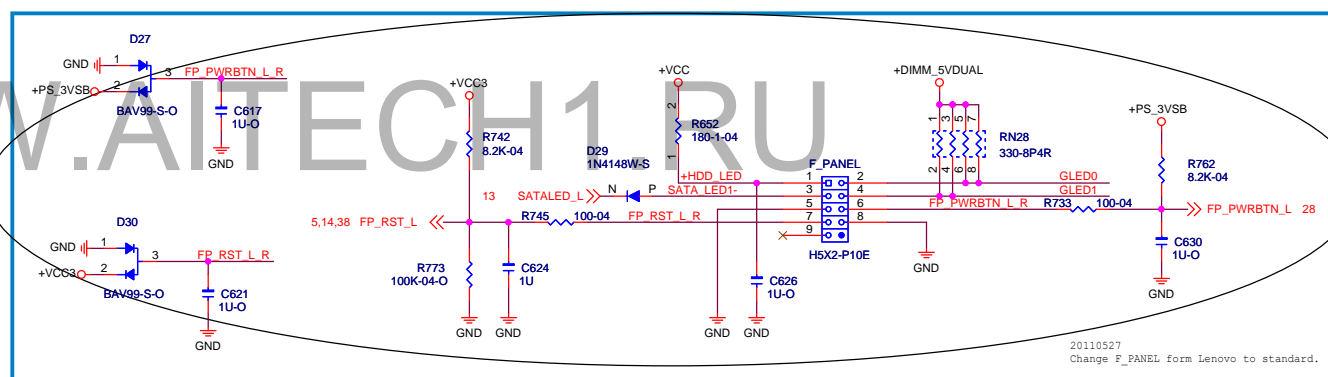
Single PS/2 Connector + 2 Ports USB2.0 Circuit



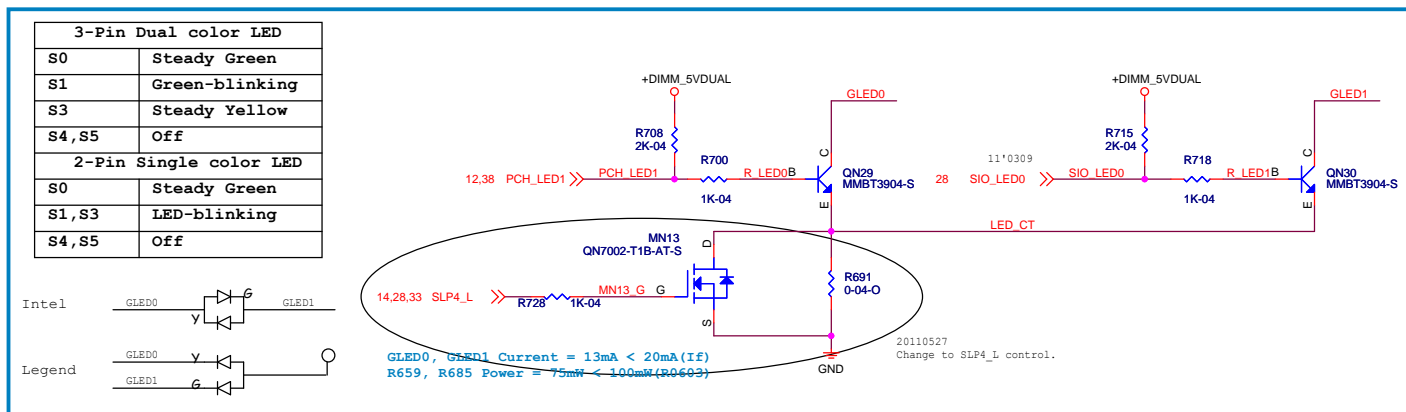
FOR CHOKE OPTION USB Discharge Circuit



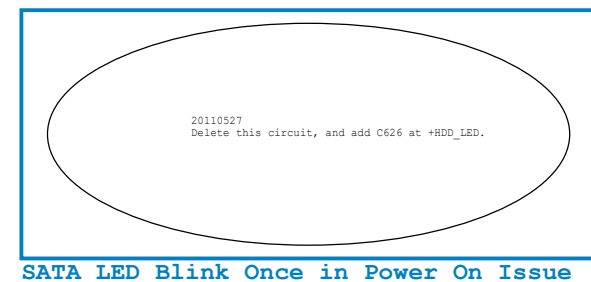
Buzzer Circuit



Front Panel Circuit



Front LED



SATA LED Blink Once in Power On Issue

EuP Lot6 2013 0.5W:

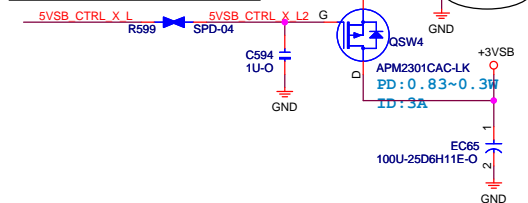
PWR STATE	+5VSB Source
S0	+PS 5VSB
S3	+PS 5VSB
S4	OFF
S5	OFF

03-050-530179
MOSFET P-CH.APM2301CAC..
Vds=-20V.Vgs=12V.Id=-3A.Rds(on)=70m OHM.
SOT-23-3.....LEAD-FREE(RoHS).ANPEC
03-050-540226(智)

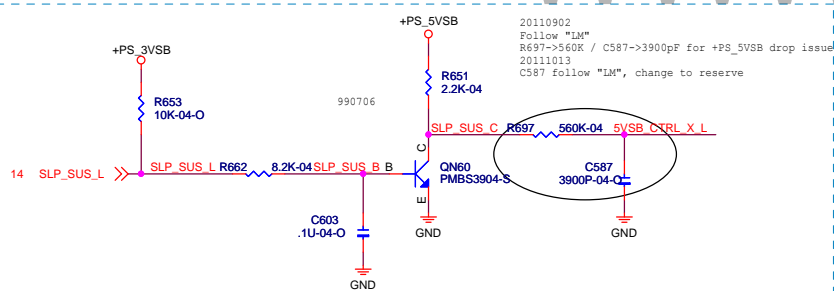
Layout Note:
Close to ATX 24P2R Connector.

EuP Lot6 2013 0.5W:

PWR STATE	+5VSB Source
S0	+PS 5VSB
S3	+PS 5VSB
S4	OFF
S5	OFF



EuP Lot6 Power Saving Circuit



11'0121
Cuz: Change to use SIO+Intel EuP Solution.
So: Add SLP_SUS_L Circuit.

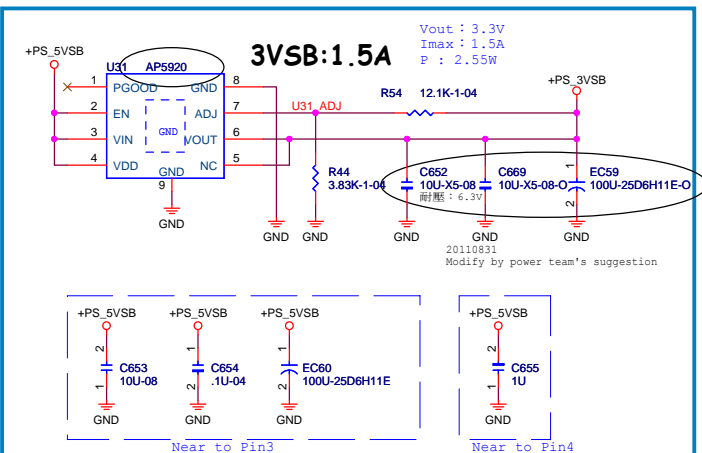
11'0210 Del PCH_MEPWROK Circuit

PCH_MEPWROK Circuit

3VSB (S0):

Power Name	Current
PCH	109mA
LAN RTL8111E-VL	165mA
SIO I18772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	1.1A
Total Current	0.28 + 2.6 = 2.88A

20111019
Change tp AP5920



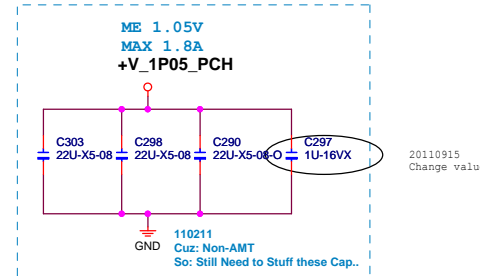
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DC/DC 3VDUAL

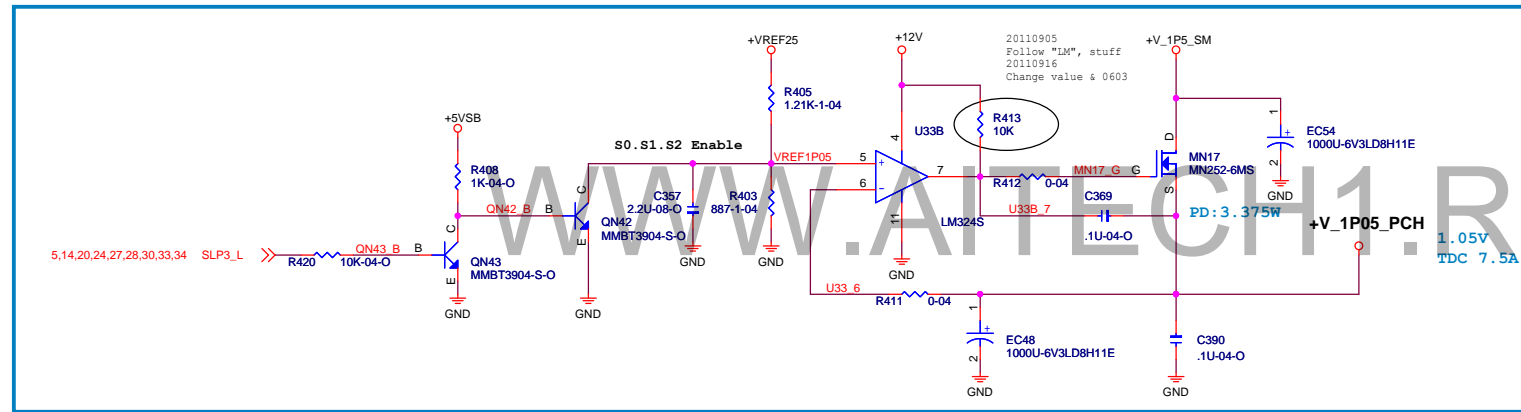
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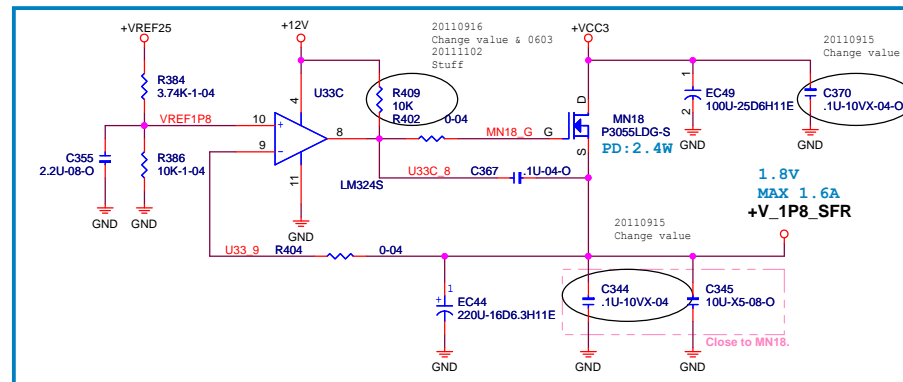
11'0210
Del +V_1P05_ME Power Circuit.



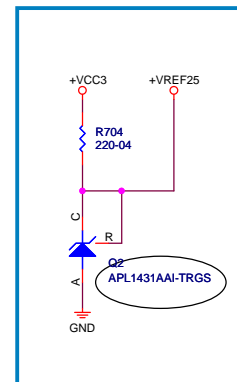
+V_1P05_ME



+V_1P05_PCH



V1P8_SFR(1.6A max)



VREF25

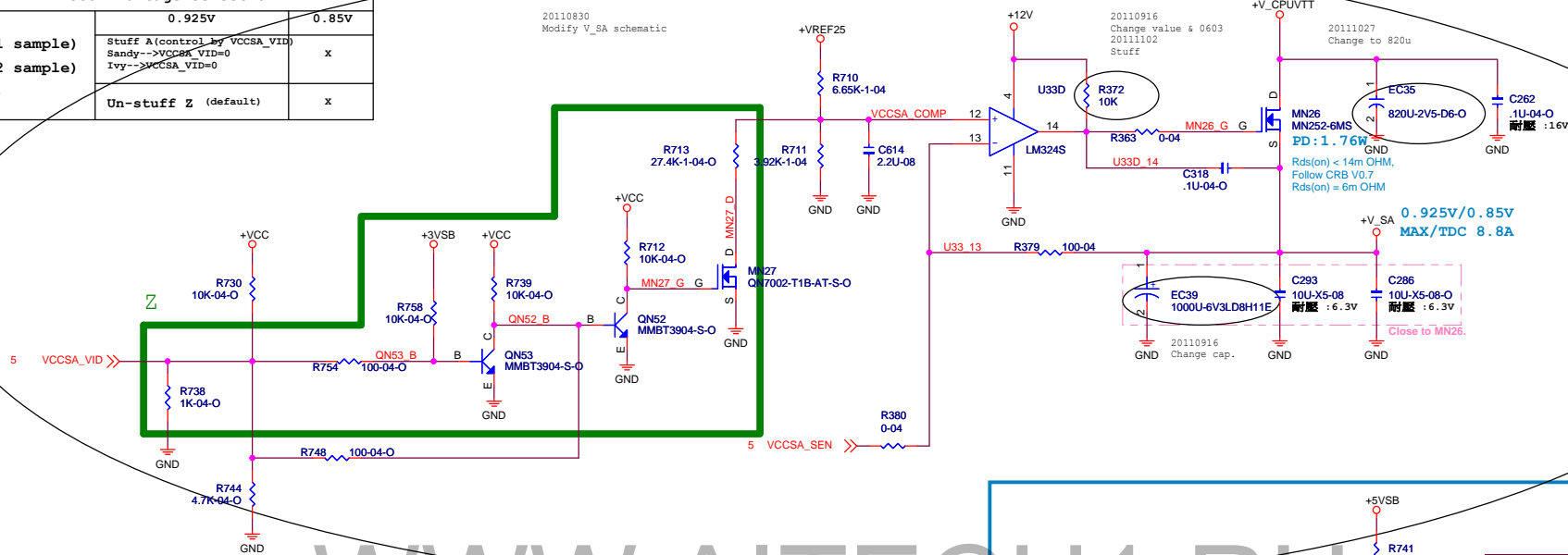
02-348-431705
Value: IC REG.APL1431AAI-TRL..SOT-23..2.5V
Footprint: SOT23_RAC_Z_2

V_SA

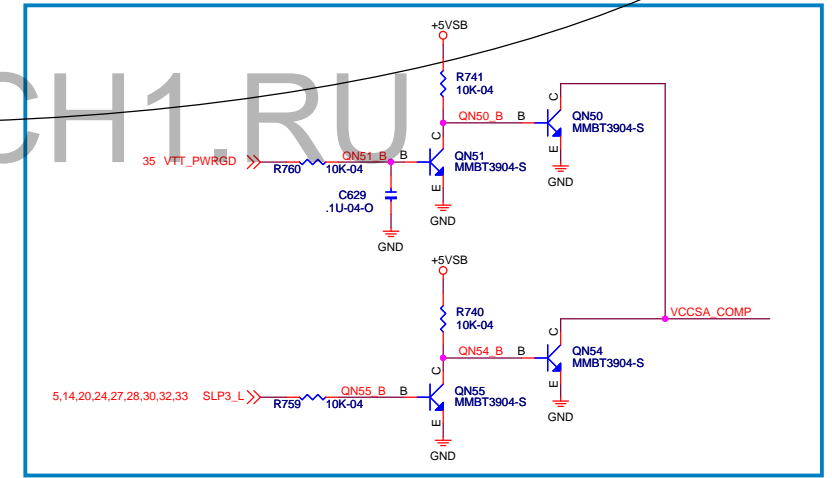
WW23 Intel POR : VCCSA=0.925V for Ivy/Sandy Bridge

VCCSA voltage selection		
	0.925V	0.85V
CPU (ES1 sample)	Stuff A (control by VCCSA_VID)	
CPU (ES2 sample)	Sandy-->VCCSA_VID=0	x
CPU (QS)	Ivy-->VCCSA_VID=0	
	Un-stuff Z (default)	x

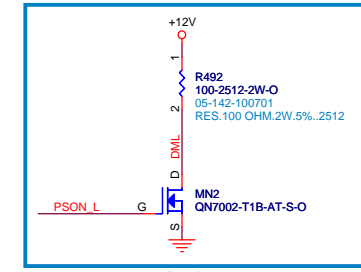
20110830
Modify V_SA schematic



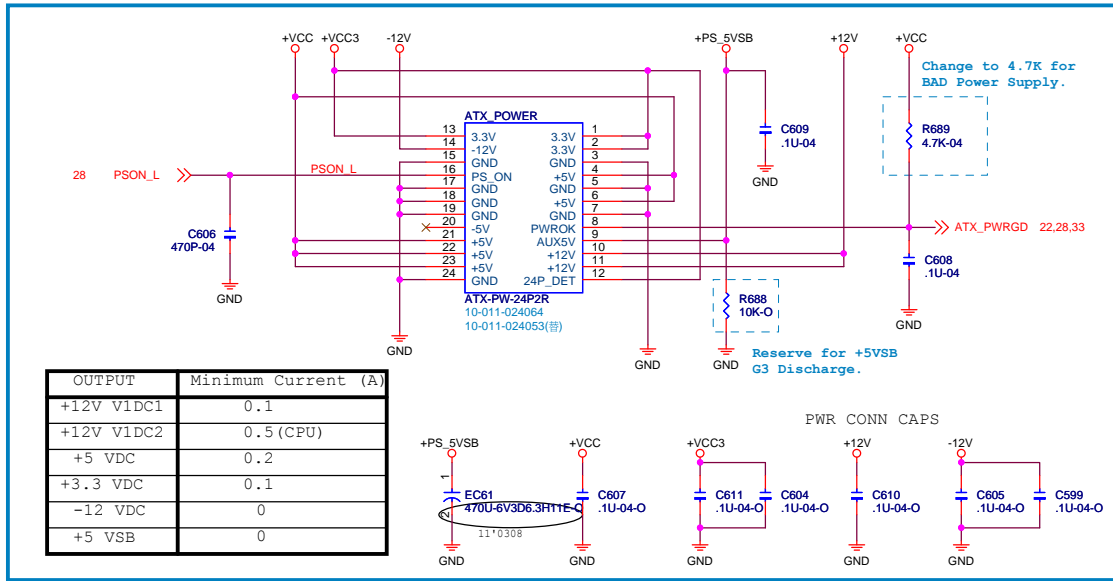
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V_SA sequence



Dummy Load for Power

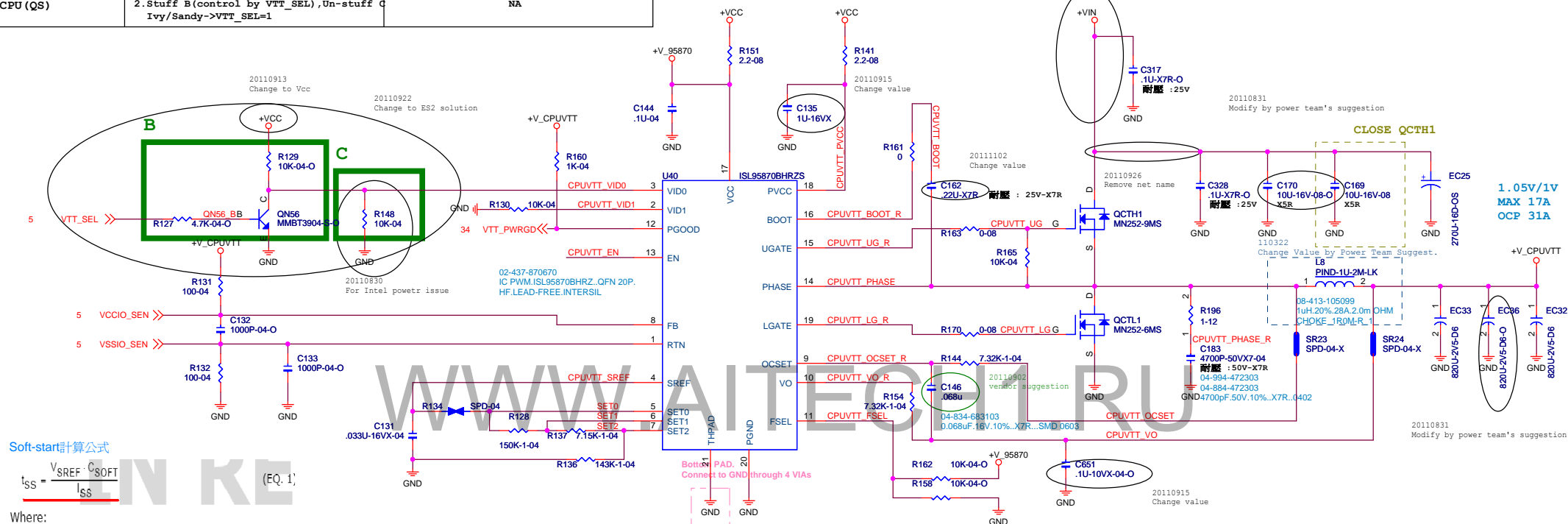


ATX Power 24PIN

WW23 Intel POR : VCCIO=1.05V for Ivy/Sandy Bridge

VCCIO voltage selection		
	1.05V	1V
CPU (ES1 sample)	Stuff B(control by VTT_SEL),Un-stuff C Sandy->VTT_SEL=1	Stuff B(control by VTT_SEL),un-stuff C Ivy->VTT_SEL=0
CPU (ES2 sample)	Un-stuff B & Stuff C	NA
CPU (QS)	1.Un-stuff B & Stuff C 2.Stuff B(control by VTT_SEL),Un-stuff C Ivy/Sandy->VTT_SEL=1	NA

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1v
high	1.05v



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad (\text{EQ. 1})$$

Where:

- I_{SS} is the soft-start current source at the 20 μ A limit
- V_{SSREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V _{SREF}	V _{OUT}
1	1	SW0	V _{SET1}	V _{OUT1}
1	0	SW1	V _{SET2}	V _{OUT2}
0	1	SW2	V _{SET3}	V _{OUT3}
0	0	SW3	V _{SET4}	V _{OUT4}

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad (EQ. 21)$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}} \right) \quad (\text{EQ. 22})$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET1}} \right) \quad (EQ. 23)$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

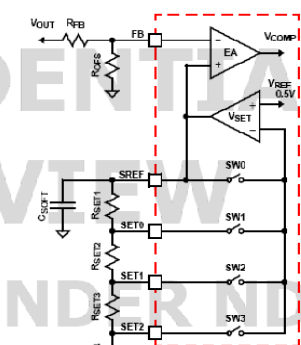
$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}} \right) \quad (\text{EQ. 24})$$


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT

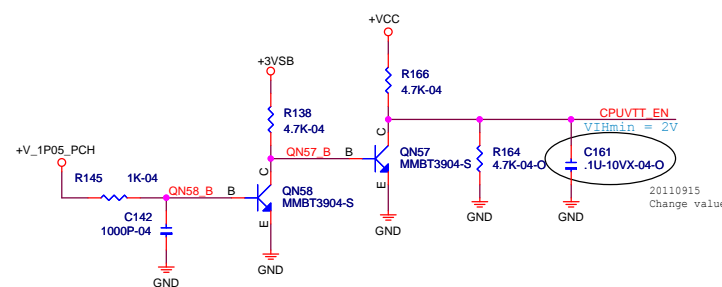
Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

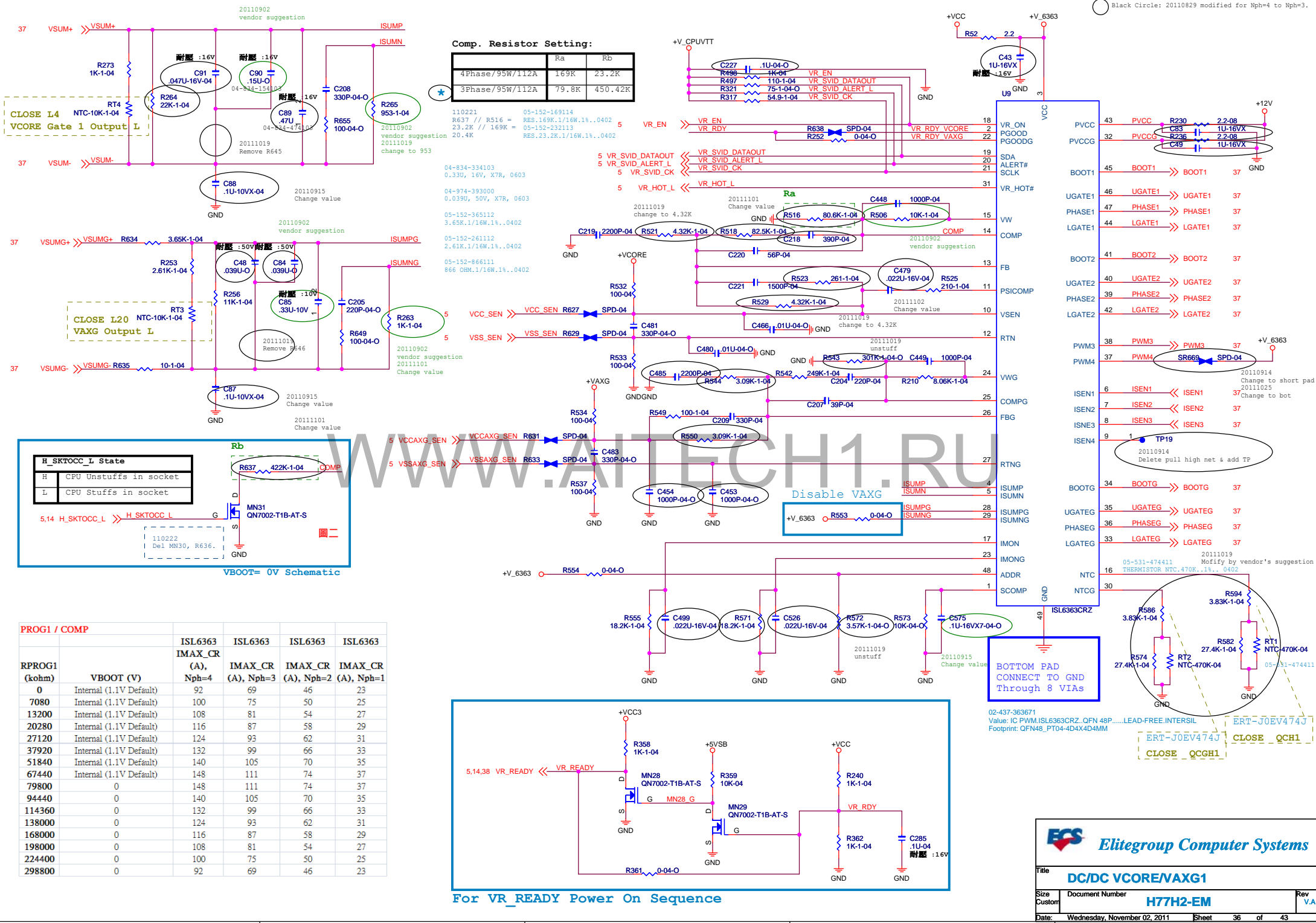
Note

- ```

1. Rocset = Iout*DCR/Iocset ; Iocset = 10uA
 If DCR = 2m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K
2. Csen = L/Rocset*DCR
 If DCR = 2m ; L = 1u, Csen = 1u/2K*1m --> Csen = 0.5u

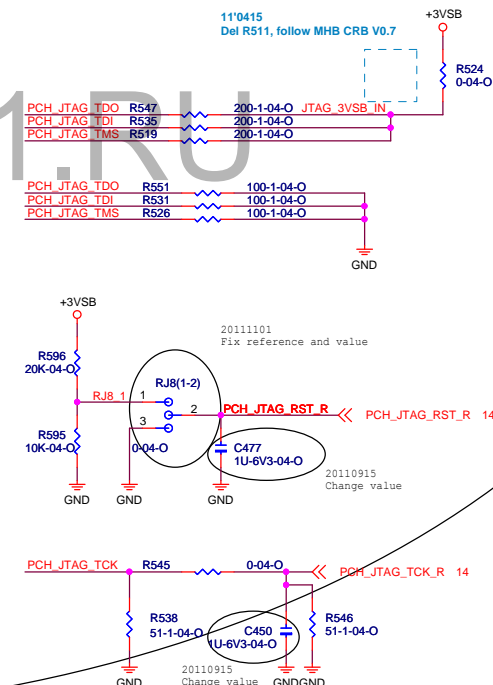
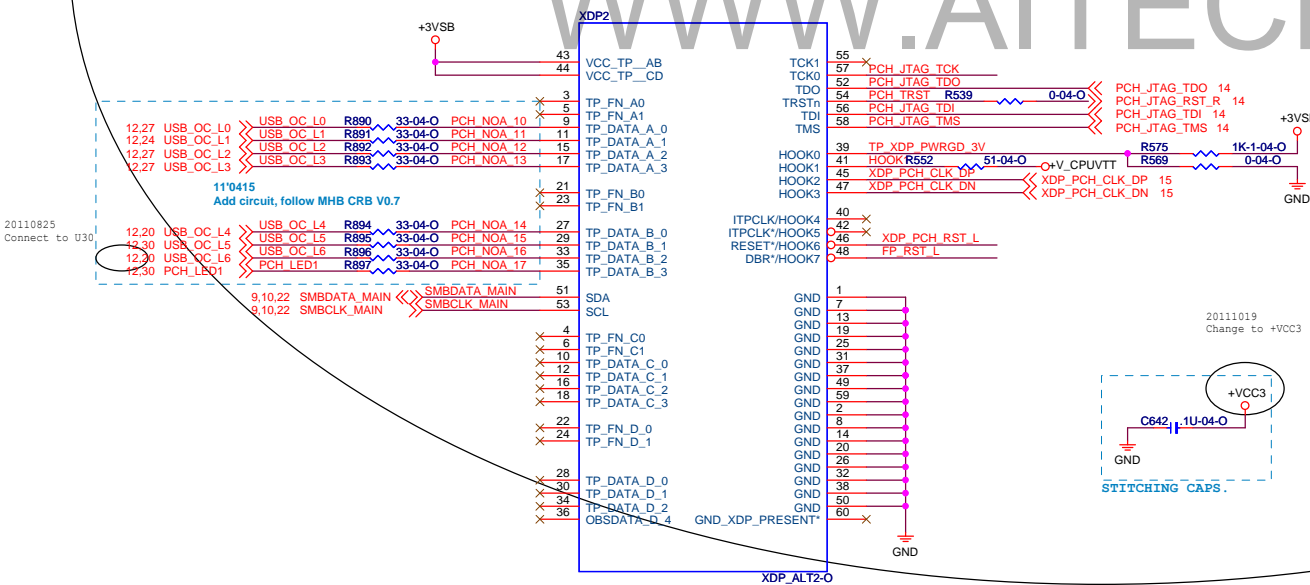
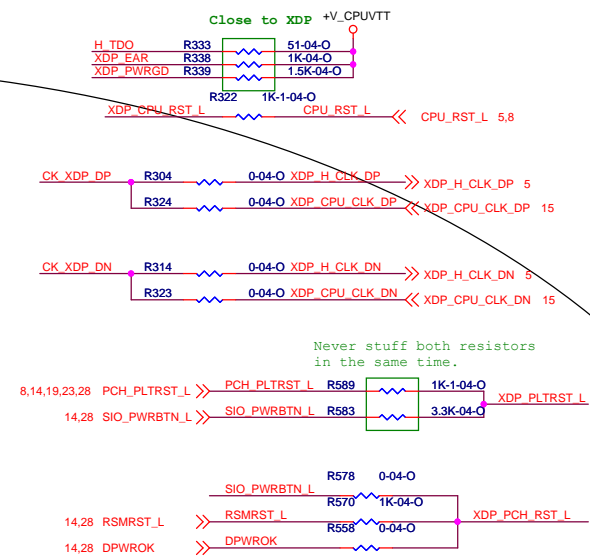
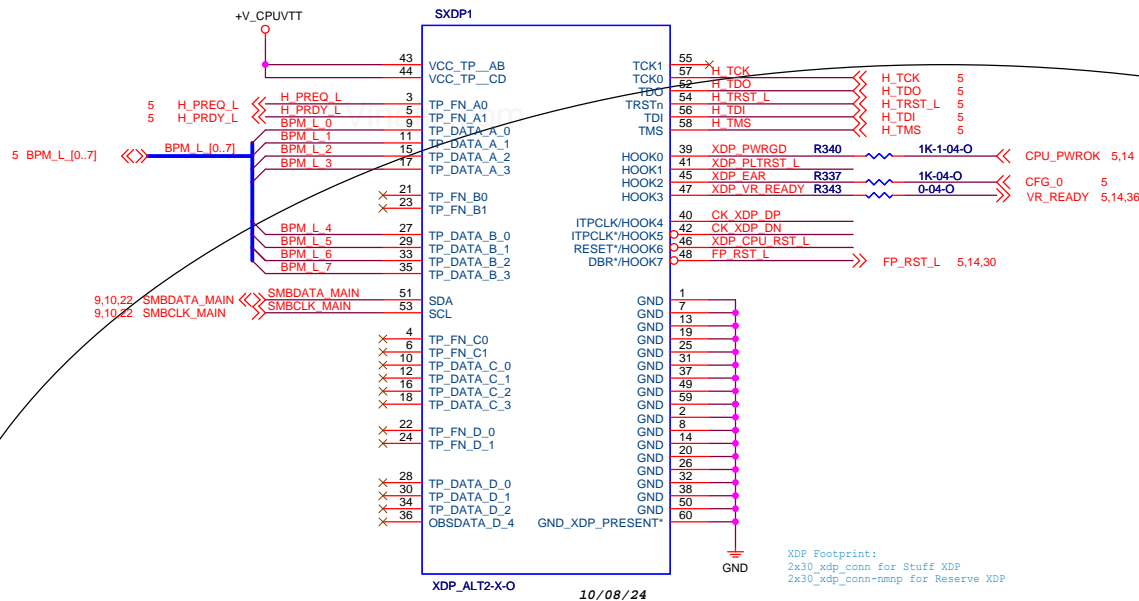
```











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PCH Strap Pin

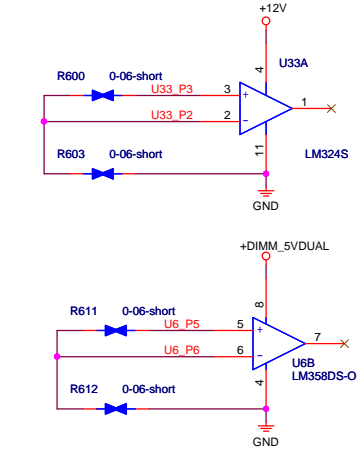
| Pin Name         | Usage                                            | Default Status                                                                                       |
|------------------|--------------------------------------------------|------------------------------------------------------------------------------------------------------|
| SPKR             | No Reboot                                        | 20K internal pull-down · No Reboot Mode with TCO Disabled:                                           |
| INIT3_3V#        | Reserved                                         | 20K internal pull-up · intend for Firmware Hub.                                                      |
| GNT[3]#/GPIO[55] | Disable Top-Block Swap                           | 20K internal pull-up · “topblock swap” mode Disable                                                  |
| INTVRMEN         | Enable Integrated 1.05V VRM                      | Need External Pull-up · Integrated 1.05V VRM Enable                                                  |
| GNT1# /GPIO51    | Boot BIOS Strap bit [1] BBS[1]                   | 20K internal pull-up · The default flash selection is the SPI flash.All                              |
| SATA1GP / GPIO19 | Boot BIOS Strap bit[0] BBS[0]                    | 20K internal pull-up · The default flash selection is the SPI flash.All                              |
| HDA_SDO          | Flash Descriptor Security Override/ ME           | Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default) |
| DF_TV5           | Enable DMI termination voltage                   | This signal has a weak internal pull-down.                                                           |
| GPIO28           | Eable On-Die PLL Voltage Regulator               | The On-Die PLL voltage regulator is enabled                                                          |
| HDA_SYNC         | On-Die PLL Voltage Regulator Voltage Select 1.8V | 20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low. |
| GPIO15           | Disable TLS Confidentiality                      | Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.  |

SIO Strap Pin

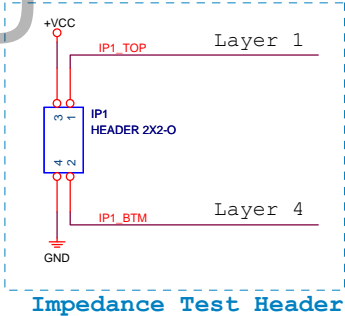
Power-On Strapping

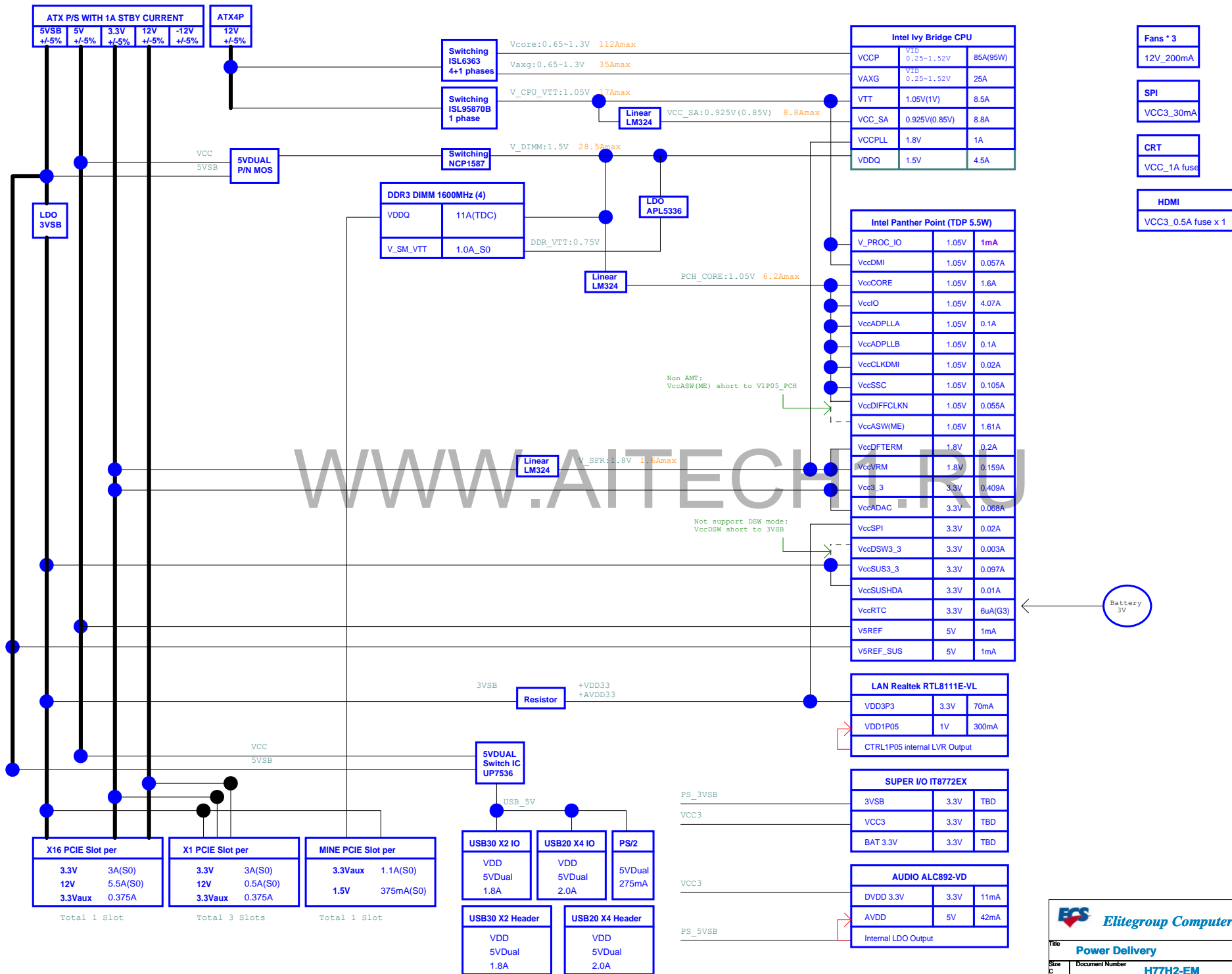
|        | Symbol      | Value | Description                         |
|--------|-------------|-------|-------------------------------------|
| JP1    | DSW_EUP_SEL | 1     | EUP(default)                        |
| Pin-23 |             | 0 *   | DSW                                 |
| JP2    | WDT_EN      | 1 *   | Disable WDT to reset PWROK(default) |
| Pin-57 |             | 0     | Enable WDT to reset PWROK           |
| JP3    | FAN_CTL_SEL | 1 *   | EC Index 6Bh/73h default = 80h      |
| Pin-59 |             | 0     | EC Index 6Bh/73h default = 00h      |
| JP4    | K8PWR_EN    | 1 *   | Disable K8 Power Sequence(default)  |
| Pin-61 |             | 0     | Enable K8 Power Sequence            |

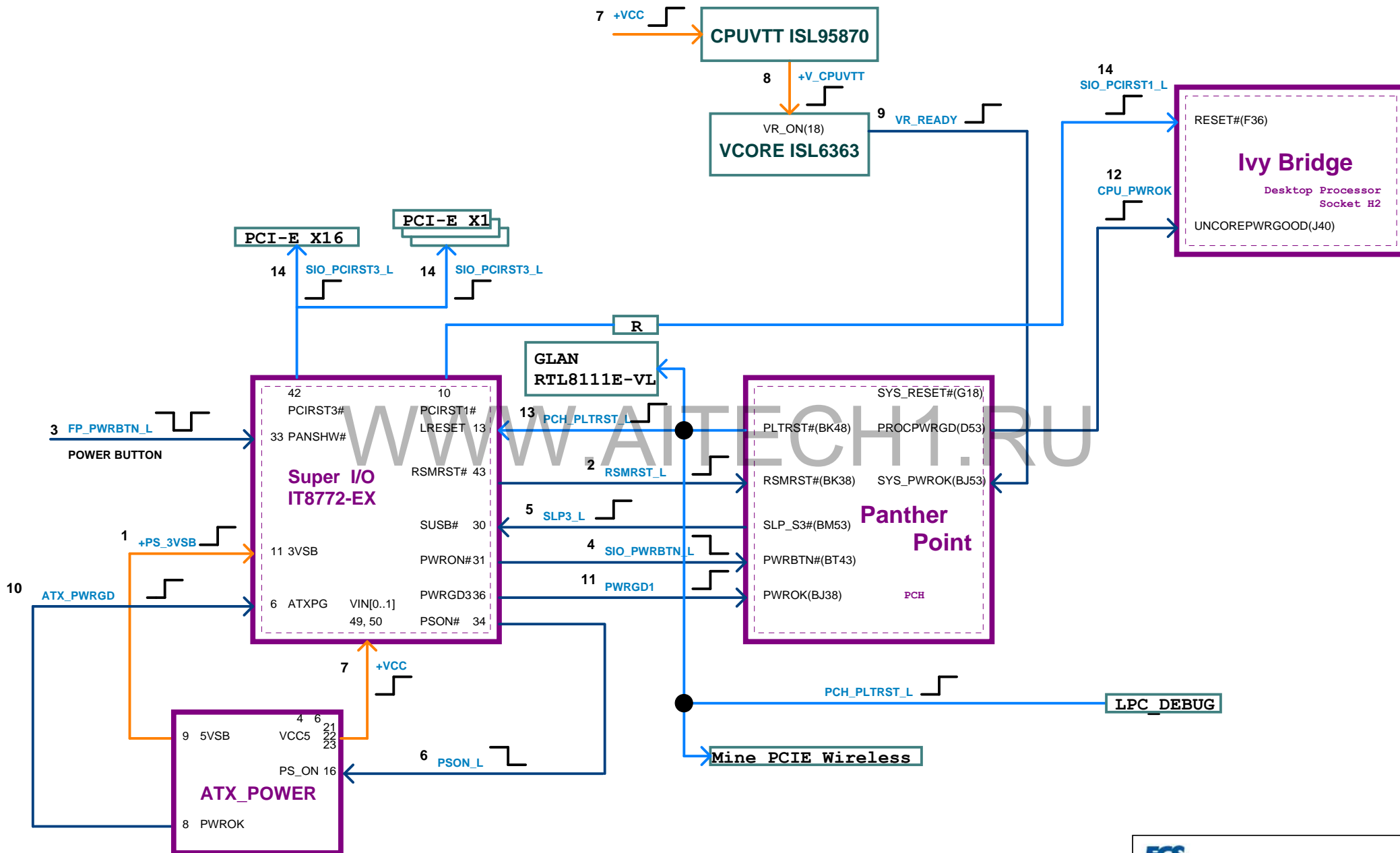
Note:  
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

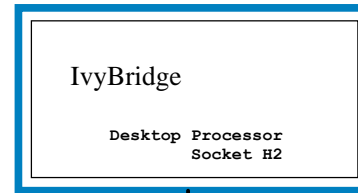


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CK\_DIMM\_A [3:0] \_H/L

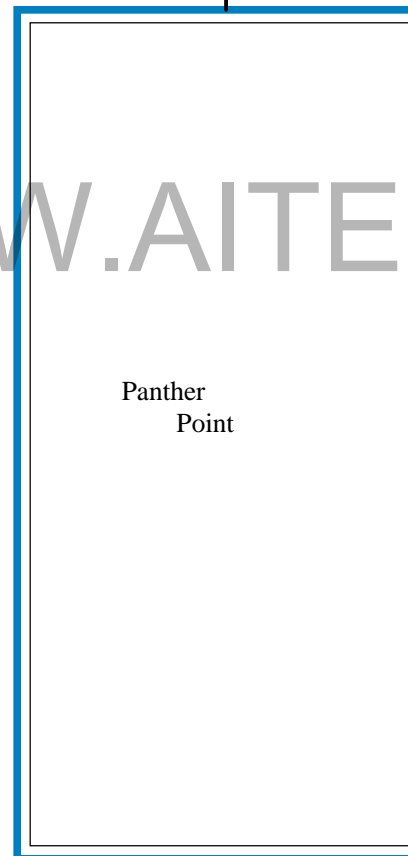
DDR3 Channel A

CK\_DIMM\_B [3:0] \_H/L

DDR3 Channel B

DDR3  
1333MHz/1066MHz

CK\_CPU\_100M\_P/N



PEX16\_100M\_P/N

PCI-E X16

PEX1[A..C]\_100M\_P/N

PCI-E X1

WLAN\_CLK\_P/N

Mini PCIE Wireless

GLAN\_CLK\_P/N

LAN  
RTL8111E-VL

XTL 25M

PCI\_33M\_FB

LDG33M

LPC\_DEBUG

SIO33M

SIO:  
IT8772

SIO48M

XTL 32.768K

XTL 25M

**ECS** Elitegroup Computer Systems

Title: **Clock Distribution**

|             |                              |                |
|-------------|------------------------------|----------------|
| Size Custom | Document Number              | Rev            |
|             | <b>H77H2-EM</b>              | <b>V.A</b>     |
| Date:       | Wednesday, November 02, 2011 | Sheet 42 of 43 |